# HA7210, HA7211

November 1996

## 10kHz to 10MHz, Low Power Crystal Oscillator

### Features

- **Single Supply Operation at 32kHz . . . . . . . . . . 2V to 7V**
- **Operating Frequency Range. . . . . . . . 10kHz to 10MHz**
- **Supply Current at 32kHz . . . . . . . . . . . . . . . . . . . . . .5μA**
- **Supply Current at 1MHz . . . . . . . . . . . . . . . . . . . .130μA**
- **Drives 2 CMOS Loads**
- **Only Requires an External Crystal for Operation**
- **Two Pinouts Available**

### Applications

- **Battery Powered Circuits**
- **Remote Metering**
- **Embedded Microprocessors**
- **Palm Top/Notebook PC**
- **Related Literature**
  - **AN9334, Improving HA7210 Start-Up Time**

### Description

The HA7210 and HA7211 are very low power crystal-controlled oscillators that can be externally programmed to operate between 10kHz and 10MHz. For normal operation it requires only the addition of a crystal. The part exhibits very high stability over a wide operating voltage and temperature range.

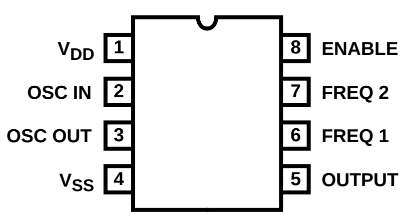
The HA7210 and HA7211 also feature a disable mode that switches the output to a high impedance state. This feature is useful for minimizing power dissipation during standby and when multiple oscillator circuits are employed.

### Ordering Information

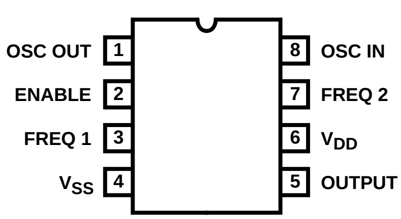
| PART NUMBER (BRAND) | TEMP. RANGE ($^oC$) | PACKAGE | PKG. NO. |
|---|---|---|---|
| HA7210IP | -40 to 85 | 8 Ld PDIP | E8.3 |
| HA7210IB (H7210I) | -40 to 85 | 8 Ld SOIC | M8.15 |
| HA7210Y | -40 to 85 | DIE | |
| HA7211IB (H7211I) | -40 to 85 | 8 Ld SOIC | M8.15 |

### Pinouts

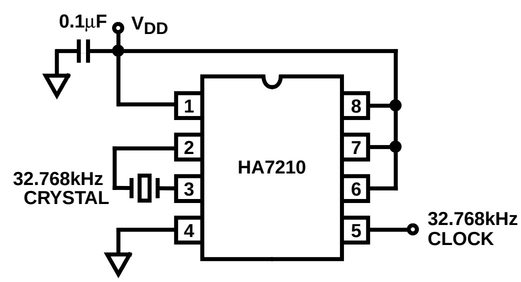
**HA7210**
**(PDIP, SOIC)**
TOP VIEW



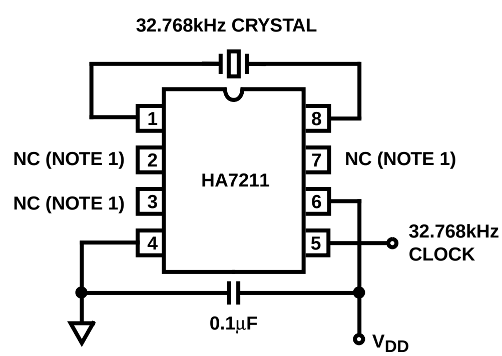

**HA7211**
**(SOIC)**
TOP VIEW




### Typical Application Circuits




**32.768kHz MICROPOWER CLOCK OSCILLATOR**

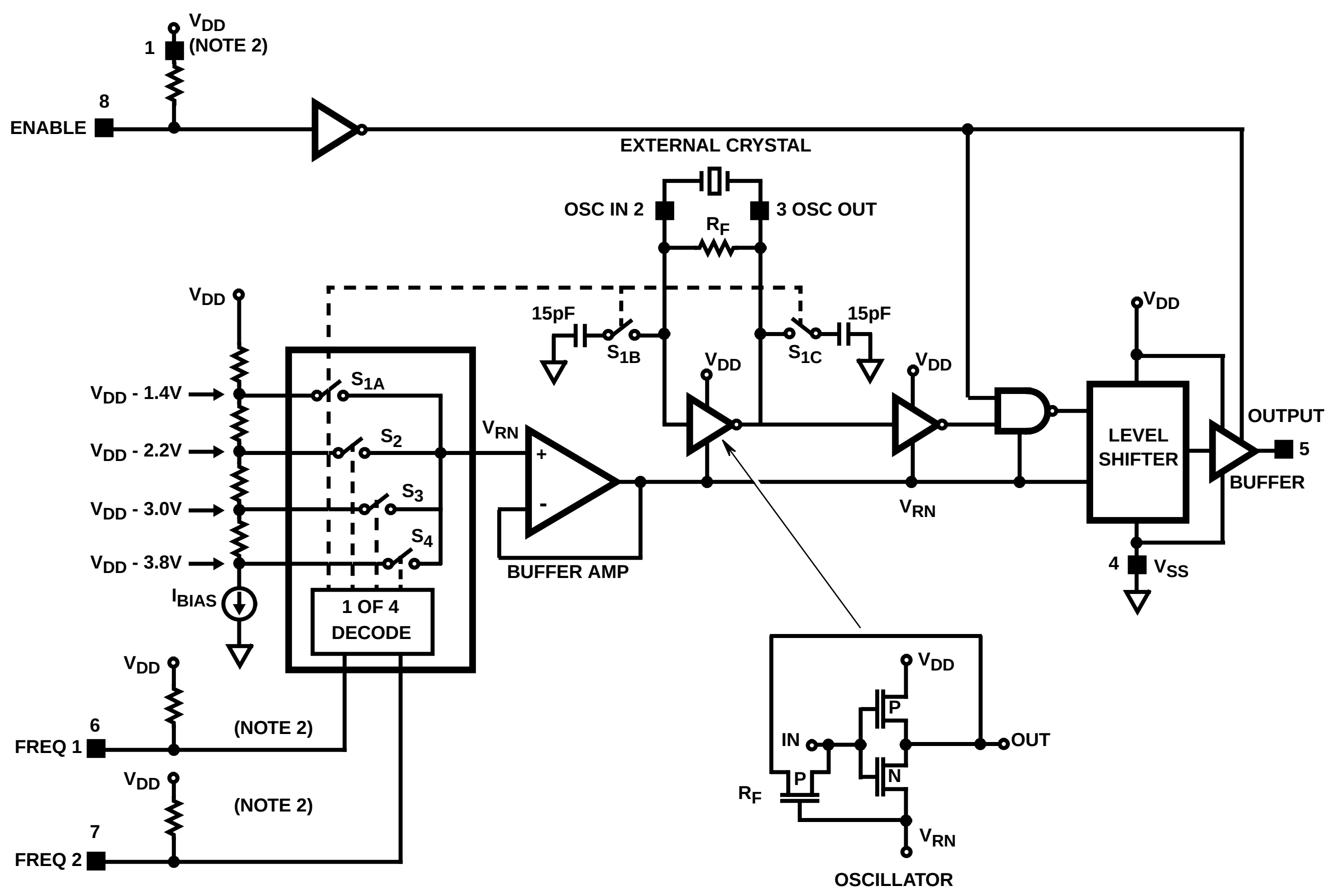



NOTE:
1. Internal pull-up resistors provided for both HA7210 and HA7211.



File Number **3389.6**

## *Simplified Block Diagram* (HA7210)




**FREQUENCY SELECTION TRUTH TABLE**

| ENABLE | FREQ 1 | FREQ 2 | SWITCH | OUTPUT RANGE |
|---|---|---|---|---|
| 1 | 1 | 1 | $S_{1A}$, $S_{1B}$, $S_{1C}$ | 10kHz - 100kHz |
| 1 | 1 | 0 | $S_2$ | 100kHz - 1MHz |
| 1 | 0 | 1 | $S_3$ | 1MHz - 5MHz |
| 1 | 0 | 0 | $S_4$ | 5MHz - 10MHz+ |
| 0 | X | X | X | High Impedance |

NOTE:

2. Logic input pull-up resistors are constant current source of 0.4μA.

## Absolute Maximum Ratings

Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10V
Voltage (any pin). . . . . . . . . . . . . . . . . . . . . $V_{SS}$-0.3V to $V_{DD}$+0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 4000V

## Operating Conditions

Temperature Range (Note 3) . . . . . . . . . . . . . . . . . . -40°C to 85°C

## Thermal Information

Thermal Resistance (Typical, Note 4) $\theta_{JA}$ (°C/W)
PDIP Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 125
SOIC Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 170
Maximum Junction Temperature (Plastic Package) . . . . . . . . 150°C
Maximum Storage Temperature Range . . . . . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

3. This product is production tested at 25°C only.
4. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications   $V_{SS}$ = GND, $T_A$ = 25°C, Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | $V_{DD}$ = 5V | | | $V_{DD}$ = 3V | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{DD}$ Supply Range | $f_{OSC}$ = 32kHz | 2 | 5 | 7 | - | - | - | V |
| $I_{DD}$ Supply Current | $f_{OSC}$ = 32kHz, EN = 0 (Standby) | - | 5.0 | 9.0 | - | - | - | µA |
| | $f_{OSC}$ = 32kHz, $C_L$ = 10pF (Note 5), EN = 1, Freq1 = 1, Freq2 = 1 | - | 5.2 | 10.2 | - | 3.6 | 6.1 | µA |
| | $f_{OSC}$ = 32kHz, $C_L$ = 40pF, EN = 1, Freq1 = 1, Freq2 = 1 | - | 10 | 15 | - | 6.5 | 9 | µA |
| | $f_{OSC}$ = 1MHz, $C_L$ = 10pF (Note 5), EN = 1, Freq1 = 0, Freq2 = 1 | - | 130 | 200 | - | 90 | 180 | µA |
| | $f_{OSC}$ = 1MHz, $C_L$ = 40pF, EN = 1, Freq1 = 0, Freq2 = 1 | - | 270 | 350 | - | 180 | 270 | µA |
| $V_{OH}$ Output High Voltage | $I_{OUT}$ = -1mA | 4.0 | 4.9 | - | - | 2.8 | - | V |
| $V_{OL}$ Output Low Voltage | $I_{OUT}$ = 1mA | - | 0.07 | 0.4 | - | 0.1 | - | V |
| $I_{OH}$ Output High Current | $V_{OUT}$ ≥ 4V | - | -10 | -5 | - | - | - | mA |
| $I_{OL}$ Output Low Current | $V_{OUT}$ ≤ 0.4V | 5.0 | 10.0 | - | - | - | - | mA |
| Three-State Leakage Current | $V_{OUT}$ = 0V, 5V, $T_A$ = 25°C, -40°C | - | 0.1 | - | - | - | - | nA |
| | $V_{OUT}$ = 0V, 5V, $T_A$ = 85°C | - | 10 | - | - | - | - | nA |
| $I_{IN}$ Enable, Freq1, Freq2 Input Current | $V_{IN}$ = $V_{SS}$ to $V_{DD}$ | - | 0.4 | 1.0 | - | - | - | µA |
| $V_{IH}$ Input High Voltage Enable, Freq1, Freq2 | | 2.0 | - | - | - | - | - | V |
| $V_{IL}$ Input Low Voltage Enable, Freq1, Freq2 | | - | - | 0.8 | - | - | - | V |
| Enable Time | $C_L$ = 18pF, $R_L$ = 1kΩ | - | 800 | - | - | - | - | ns |
| Disable Time | $C_L$ = 18pF, $R_L$ = 1kΩ | - | 90 | - | - | - | - | ns |
| $t_R$ Output Rise Time | 10% - 90%, $f_{OSC}$ = 32kHz, $C_L$ = 40pF | - | 12 | 25 | - | 12 | - | ns |
| $t_F$ Output Fall Time | 10% - 90%, $f_{OSC}$ = 32kHz, $C_L$ = 40pF | - | 12 | 25 | - | 14 | - | ns |
| Duty Cycle, Packaged Part Only (Note 6) | $C_L$ = 40pF, $f_{OSC}$ = 1MHz | 40 | 54 | 60 | - | - | - | % |
| Duty Cycle, (See Typical Curves) | $C_L$ = 40pF, $f_{OSC}$ = 32kHz | - | 41 | - | - | 44 | - | % |
| Frequency Stability vs Supply Voltage | $f_{OSC}$ = 32kHz, $V_{DD}$ = 5V, $C_L$=10pF | - | 1 | - | - | - | - | ppm/V |
| Frequency Stability vs Temperature | $f_{OSC}$ = 32kHz, $V_{DD}$ = 5V, $C_L$=10pF | - | 0.1 | - | - | - | - | ppm/°C |
| Frequency Stability vs Load | $f_{OSC}$ = 32kHz, $V_{DD}$ = 5V, $C_L$=10pF | - | 0.01 | - | - | - | - | ppm/pF |

NOTES:

5. Calculated using the equation $I_{DD} = I_{DD}$ (No Load) + ($V_{DD}$) ($f_{OSC}$)($C_L$)
6. Duty cycle will vary with supply voltage, oscillation frequency, and parasitic capacitance on the crystal pins.

## Test Circuit

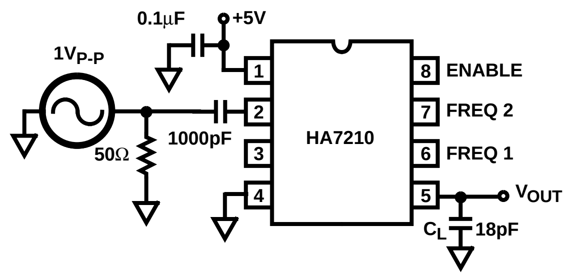



FIGURE 1.

In production the HA7210 is tested with a 32kHz and a 1MHz crystal. However for characterization purposes data was taken using a sinewave generator as the frequency determining element, as shown in Figure 1. The $1V_{P-P}$ input is a smaller amplitude than what a typical crystal would generate so the transitions are slower. In general the Generator data will show a "worst case" number for $I_{DD}$, duty cycle, and rise/fall time. The Generator test method is useful for testing a variety of frequencies quickly and provides curves which can be used for understanding performance trends. Data for the HA7210 using crystals has also been taken. This data has been overlaid onto the generator data to provide a reference for comparison.

## Application Information

### Theory Of Operation

The HA7210 and HA7211 are Pierce Oscillators optimized for low power consumption, requiring no external components except for a bypass capacitor and a Parallel Mode Crystal. The Simplified Block Diagram shows the Crystal attached to pins 2 and 3, (HA7210) the Oscillator input and output. The crystal drive circuitry is detailed showing the simple CMOS inverter stage and the P-channel device being used as biasing resistor $R_F$. The inverter will operate mostly in its linear region increasing the amplitude of the oscillation until limited by its transconductance and voltage rails, $V_{DD}$ and $V_{RN}$. The inverter is self biasing using $R_F$ to center the oscillating waveform at the input threshold. Do not interfere with this bias function with external loads or excessive leakage on pin 2 for HA7210, pin 8 for HA7211. Nominal value for $R_F$ is 17MΩ in the lowest frequency range to 7MΩ in the highest frequency range.

The HA7210 and HA7211 optimizes its power for 4 frequency ranges selected by digital inputs Freq1 and Freq2 as shown in the Block Diagram. Internal pull up resistors (constant current 0.4µA) on Enable, Freq1 and Freq2 allow the user simply to leave one or all digital inputs not connected for a corresponding "1" state. All digital inputs may be left open for 10kHz to 100kHz operation.

A current source develops 4 selectable reference voltages through series resistors. The selected voltage, $V_{RN}$, is buffered and used as the negative supply rail for the oscillator section of the circuit. The use of a current source in the reference string allows for wide supply variation with minimal effect on performance. The reduced operating voltage of the oscillator section reduces power consumption and limits transconductance and bandwidth to the frequency range selected. For frequencies at the edge of a range, the higher range may provide better performance.

The OSC OUT waveform on pin 3 for HA7210 (pin 1 for HA7211) is squared up through a series of inverters to the output drive stage. The Enable function is implemented with a NAND gate in the inverter string, gating the signal to the level shifter and output stage. Also during Disable the output is set to a high impedance state useful for minimizing power during standby and when multiple oscillators are OR'ed to a single node.

### Design Considerations

The low power CMOS transistors are designed to consume power mostly during transitions. Keeping these transitions short requires a good decoupling capacitor as close as possible to the supply pins 1 and 4 for HA7210, pins 4 and 6 for HA7211. A ceramic 0.1µF is recommended. Additional supply decoupling on the circuit board with 1µF to 10µF will further reduce overshoot, ringing and power consumption. The HA7210, when compared to a crystal and inverter alone, will speed clock transition times, reducing power consumption of all CMOS circuitry run from that clock.

Power consumption may be further reduced by minimizing the capacitance on moving nodes. The majority of the power will be used in the output stage driving the load. Minimizing the load and parasitic capacitance on the output, pin 5, will play the major role in minimizing supply current. A secondary source of wasted supply current is parasitic or crystal load capacitance on pins 2 and 3 for HA7210, pins 1 and 8 for HA7211. The HA7210 is designed to work with most available crystals in its frequency range with no external components required. Two 15pF capacitors are internally switched onto crystal pins 2 and 3 on the HA7210 to compensate the oscillator in the 10kHz to 100kHz frequency range.

The supply current of the HA7210 and HA7211 may be approximately calculated from the equation:

$$I_{DD} = I_{DD}(\text{Disabled}) + V_{DD} \times f_{OSC} \times C_L$$

where: $I_{DD}$ = Total supply current
$V_{DD}$ = Total voltage from $V_{DD}$ (pin1) to $V_{SS}$ (pin4)
$f_{OSC}$ = Frequency of Oscillation
$C_L$ = Output (pin5) load capacitance

**Example #1:**

$V_{DD}$ = 5V, $f_{OSC}$ = 100kHz, $C_L$ = 30pF
$I_{DD}$(Disabled) = 4.5µA (Figure 10)
$I_{DD}$ = 4.5µA + (5V)(100kHz)(30pF) = 19.5µA
Measured $I_{DD}$ = 20.3µA

**Example #2:**

$V_{DD}$ = 5V, $f_{OSC}$ = 5MHz, $C_L$ = 30pF
$I_{DD}$(Disabled) = 75µA (Figure 9)
$I_{DD}$ = 75µA + (5V)(5MHz)(30pF) = 825µA
Measured $I_{DD}$ = 809µA

## Crystal Selection

For general purpose applications, a Parallel Mode Crystal is a good choice for use with the HA7210 or HA7211. However for applications where a precision frequency is required, the designer needs to consider other factors.

Crystals are available in two types or modes of oscillation, Series and Parallel. Series Mode crystals are manufactured to operate at a specified frequency with zero load capacitance and appear as a near resistive impedance when oscillating. Parallel Mode crystals are manufactured to operate with a specific capacitive load in series, causing the crystal to operate at a more inductive impedance to cancel the load capacitor. Loading a crystal with a different capacitance will "pull" the frequency off its value.

The HA7210 and HA7211 has 4 operating frequency ranges. The higher three ranges do not add any loading capacitance to the oscillator circuit. The lowest range, 10kHz to 100kHz, automatically switches in two 15pF capacitors onto OSC IN and OSC OUT to eliminate potential start-up problems. These capacitors create an effective crystal loading capacitor equal to the series combination of these two capacitors. For the HA7210 and HA7211, in the lowest range, the effective loading capacitance is 7.5pF. Therefore the choice for a crystal, in this range, should be a Parallel Mode crystal that requires a 7.5pF load.

In the higher 3 frequency ranges, the capacitance on OSC IN and OSC OUT will be determined by package and layout parasitics, typically 4 to 5pF. Ideally the choice for crystal should be a Parallel Mode set for 2.5pF load. A crystal manufactured for a different load will be "pulled" from its nominal frequency (see Crystal Pullability).

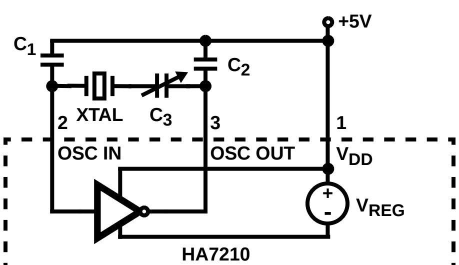



FIGURE 2.

## Frequency Fine Tuning

Two Methods will be discussed for fine adjustment of the crystal frequency. The first and preferred method (Figure 2), provides better frequency accuracy and oscillator stability than method two (Figure 3). Method one also eliminates start-up problems sometimes encountered with 32kHz tuning fork crystals.

For best oscillator performance, two conditions must be met: the capacitive load must be matched to both the inverter and crystal to provide ideal conditions for oscillation, and the frequency of the oscillator must be adjustable to the desired frequency. In Method two these two goals can be at odds with each other; either the oscillator is trimmed to frequency by de-tuning the load circuit, or stability is increased at the expense of absolute frequency accuracy.

Method one allows these two conditions to be met independently. The two fixed capacitors, $C_1$ and $C_2$, provide the optimum load to the oscillator and crystal. $C_3$ adjusts the frequency at which the circuit oscillates without appreciably changing the load (and thus the stability) of the system. Once a value for $C_3$ has been determined for the particular type of crystal being used, it could be replaced with a fixed capacitor. For the most precise control over oscillator frequency, $C_3$ should remain adjustable.

This three capacitor tuning method will be more accurate and stable than method two and is recommended for 32kHz tuning fork crystals; without it they may leap into an overtone mode when power is initially applied.

Method two has been used for many years and may be preferred in applications where cost or space is critical. Note that in both cases the crystal loading capacitors are connected between the oscillator and $V_{DD}$; do not use $V_{SS}$ as an AC ground. The Simplified Block Diagram shows that the oscillating inverter does not directly connect to $V_{SS}$ but is referenced to $V_{DD}$ and $V_{RN}$. Therefore $V_{DD}$ is the best AC ground available.

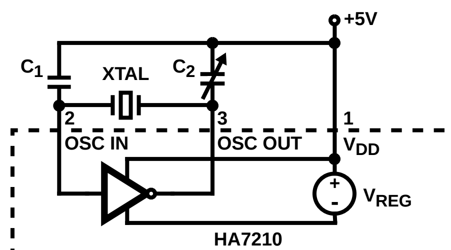



FIGURE 3.

Typical values of the capacitors in Figure 2 are shown below. Some trial and error may be required before the best combination is determined. The values listed are total capacitance including parasitic or other sources. Remember that in the 10kHz to 100kHz frequency range setting the HA7210 switches in two internal 15pF capacitors.

| CRYSTAL FREQUENCY | LOAD CAPS $C_1$, $C_2$ | TRIMMER CAP $C_3$ |
|---|---|---|
| 32kHz | 33pF | 5pF to 50pF |
| 1MHz | 33pF | 5pF to 50pF |
| 2MHz | 25pF | 5pF to 50pF |
| 4MHz | 22pF | 5pF to 100pF |

### CRYSTAL PULLABILITY

Figure 4 shows the basic equivalent circuit for a crystal and its loading circuit.

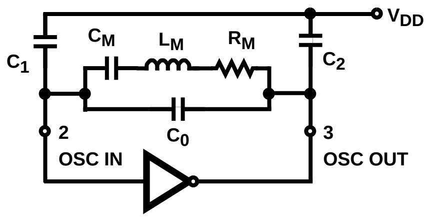



FIGURE 4.

Where: $C_M$ = Motional Capacitance
$L_M$ = Motional Inductance
$R_M$ = Motional Resistance
$C_0$ = Shunt Capacitance

$$C_{CL} = \frac{1}{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)} = \text{Equivalent Crystal Load}$$

If loading capacitance is connected to a Series Mode Crystal, the new Parallel Mode frequency of resonance may be calculated with the following equation:

$$f_P = f_S\left[1 + \frac{C_M}{2(C_0 + C_{CL})}\right]$$

Where: $f_P$ = Parallel Mode Resonant Frequency
$f_S$ = Series Mode Resonant Frequency

In a similar way, the Series Mode resonant frequency may be calculated from a Parallel Mode crystal and then you may calculate how much the frequency will "pull" with a new load.

### Layout Considerations

Due to the extremely low current (and therefore high impedance) the circuit board layout of the HA7210 or HA7211 must be given special attention. Stray capacitance should be minimized. Keep the oscillator traces on a single layer of the PCB. Avoid putting a ground plane above or below this layer. The traces between the crystal, the capacitors, and the OSC pins should be as short as possible. Completely surround the oscillator components with a thick trace of $V_{DD}$ to minimize coupling with any digital signals. The final assembly must be free from contaminants such as solder flux, moisture, or any other potential source of leakage. A good solder mask will help keep the traces free of moisture and contamination over time.

## Further Reading

Al Little "HA7210 Low Power Oscillator: Micropower Clock Oscillator and Op Amps Provide System Shutdown for Battery Circuits". Harris Semiconductor Application Note AN9317.

Robert Rood "Improving Start-Up Time at 32KHz for the HA7210 Low Power Crystal Oscillator". Harris Semiconductor Application Note AN9334.

S. S. Eaton "Timekeeping Advances Through COS/MOS Technology". Harris Semiconductor Application Note ICAN-6086.

E. A. Vittoz, et. al. "High-Performance Crystal Oscillator circuits: Theory and Application". IEEE Journal of Solid-State Circuits, Vol. 23, No3, June 1988, pp774-783.

M. A. Unkrich, et. al. "Conditions for Start-Up in Crystal Oscillators". IEEE Journal of Solid-State Circuits, Vol. 17, No1, Feb. 1982, pp87-90.

Marvin E. Frerking "Crystal Oscillator Design and Temperature Compensation". New York: Van Nostrand-Reinhold, 1978. Pierce Oscillators Discussed pp56-75.

## Typical Performance Curves

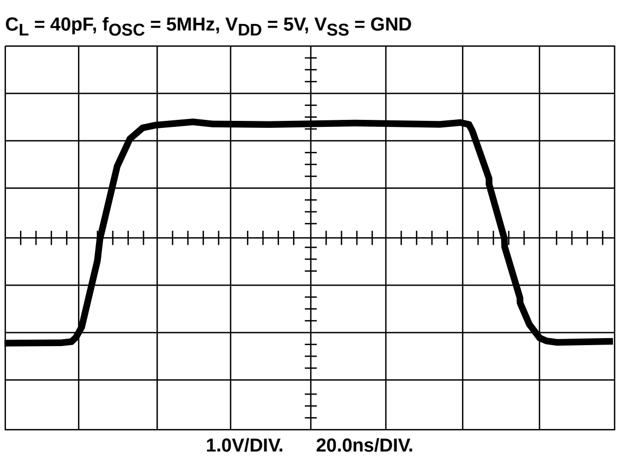



FIGURE 5. OUTPUT WAVEFORM ($C_L$ = 40pF)

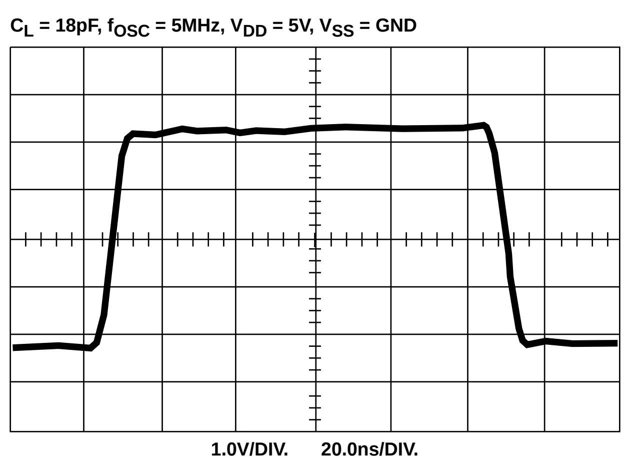



FIGURE 6. OUTPUT WAVEFORM ($C_L$ = 18pF)

NOTE: Refer to Test Circuit (Figure 1).

## *Typical Performance Curves* (Continued)

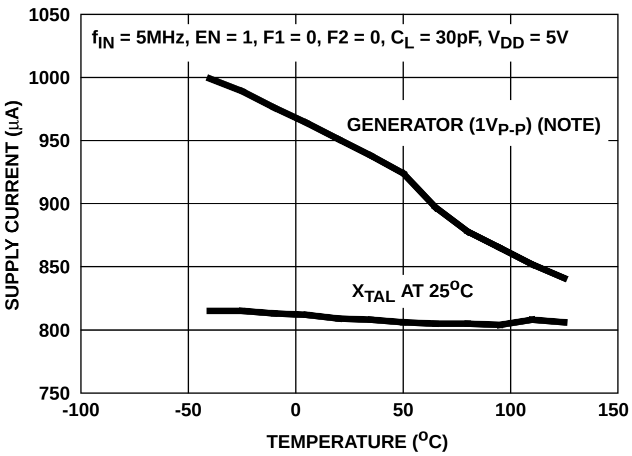



FIGURE 7. SUPPLY CURRENT vs TEMPERATURE

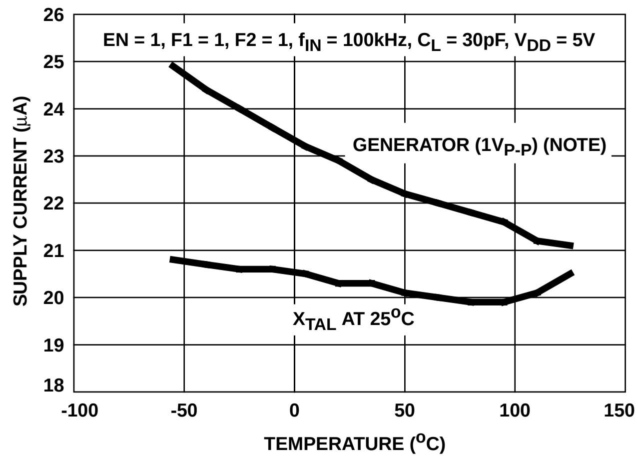



FIGURE 8. SUPPLY CURRENT vs TEMPERATURE

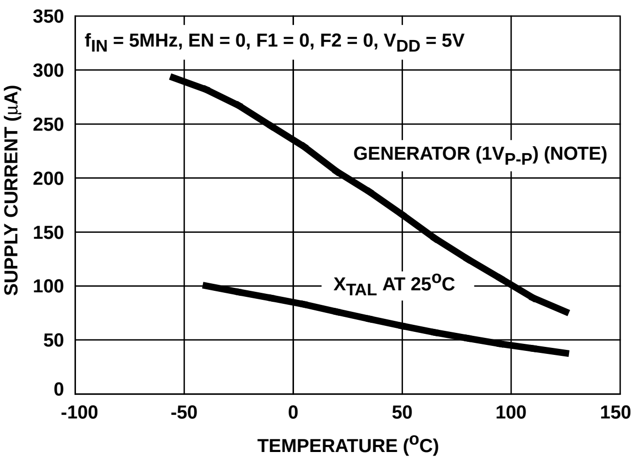



FIGURE 9. DISABLE SUPPLY CURRENT vs TEMPERATURE

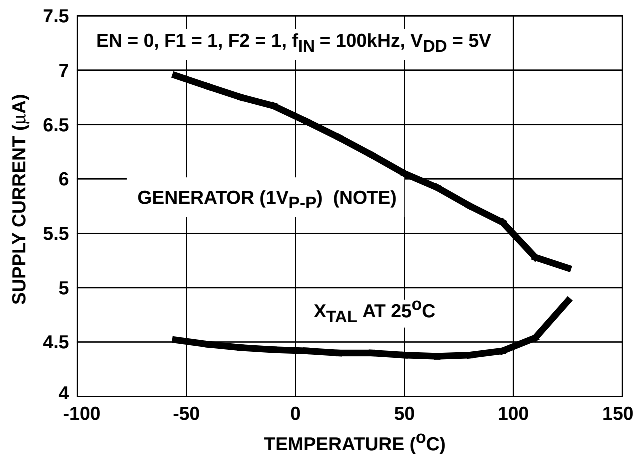



FIGURE 10. DISABLE SUPPLY CURRENT vs TEMPERATURE

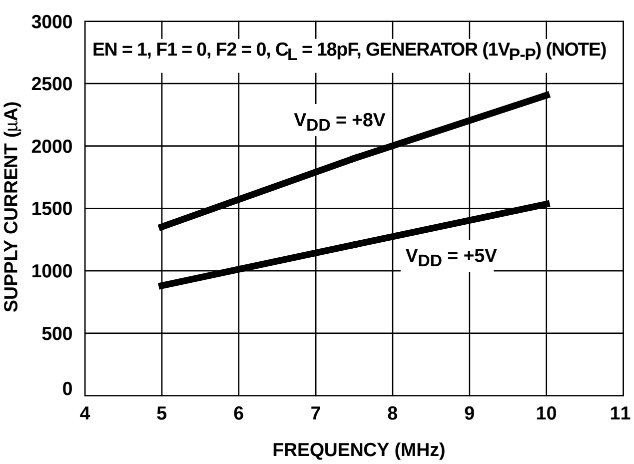



FIGURE 11. SUPPLY CURRENT vs FREQUENCY

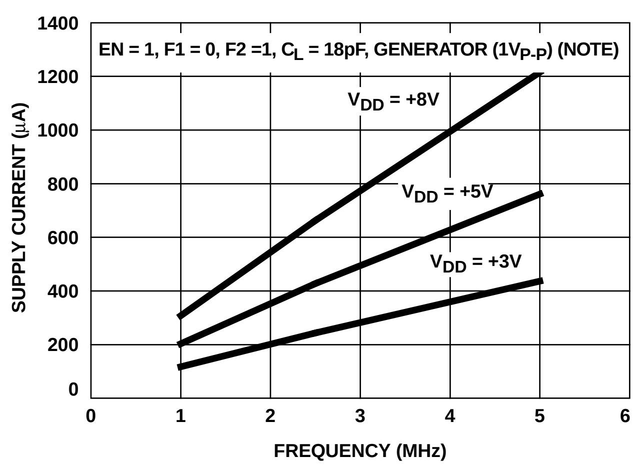



FIGURE 12. SUPPLY CURRENT vs FREQUENCY

NOTE: Refer to Test Circuit (Figure 1).

## *Typical Performance Curves* (Continued)

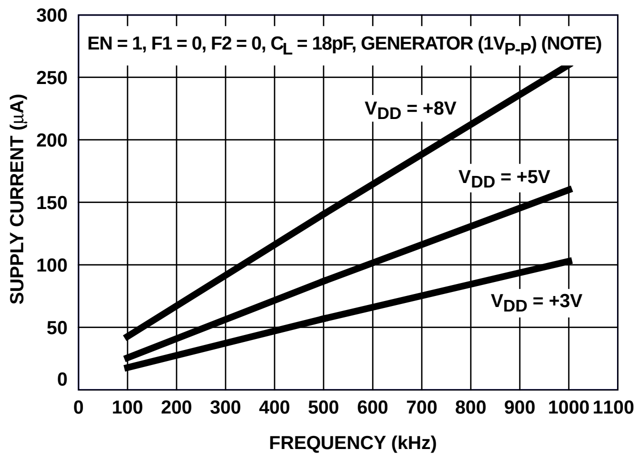



FIGURE 13. SUPPLY CURRENT vs FREQUENCY

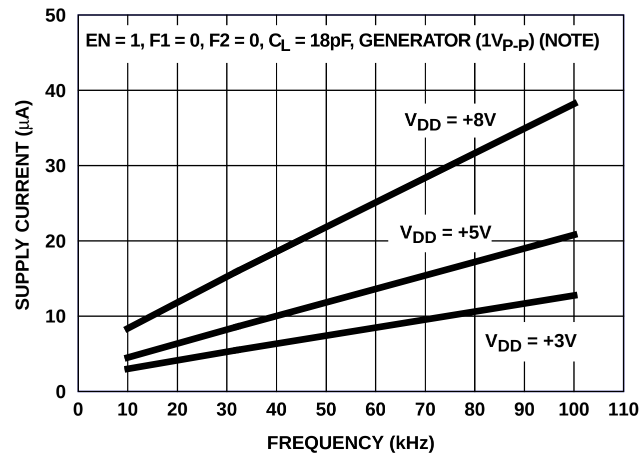



FIGURE 14. SUPPLY CURRENT vs FREQUENCY

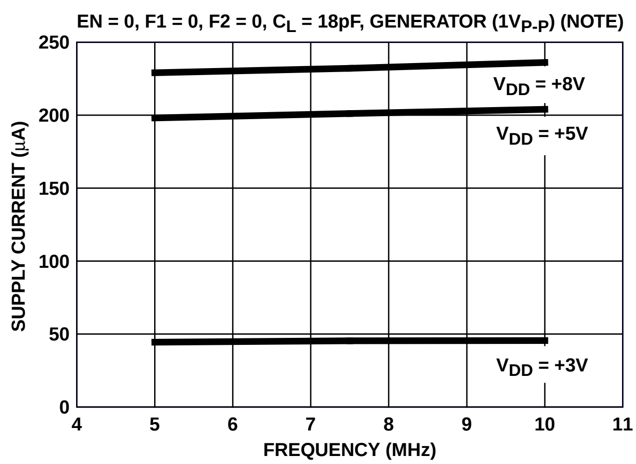



FIGURE 15. DISABLED SUPPLY CURRENT vs FREQUENCY

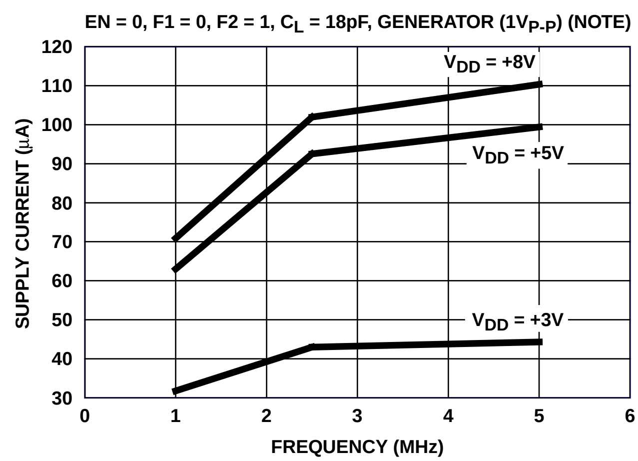



FIGURE 16. DISABLE SUPPLY CURRENT vs FREQUENCY

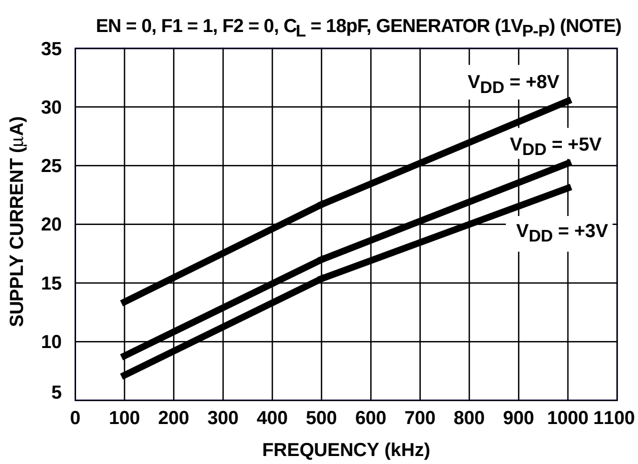



FIGURE 17. DISABLE SUPPLY CURRENT vs FREQUENCY

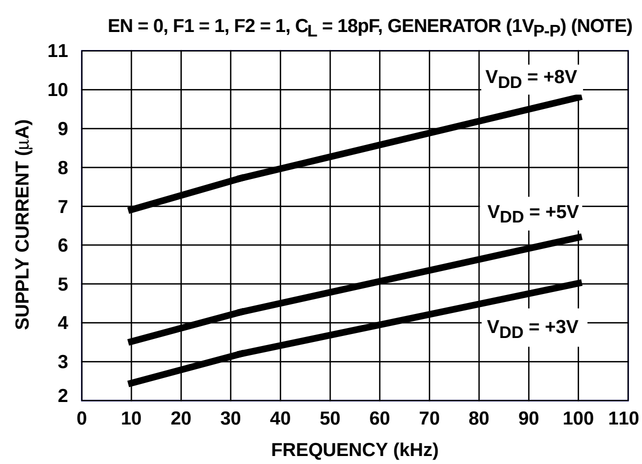



FIGURE 18. DISABLE SUPPLY CURRENT vs FREQUENCY

NOTE: Refer to Test Circuit (Figure 1).

## *Typical Performance Curves* (Continued)

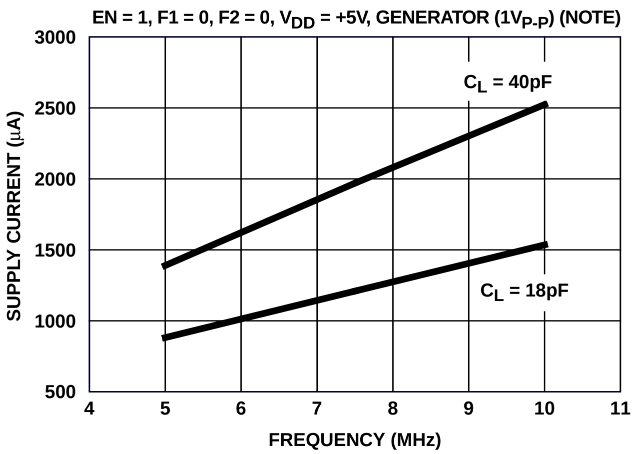



FIGURE 19. SUPPLY CURRENT vs FREQUENCY

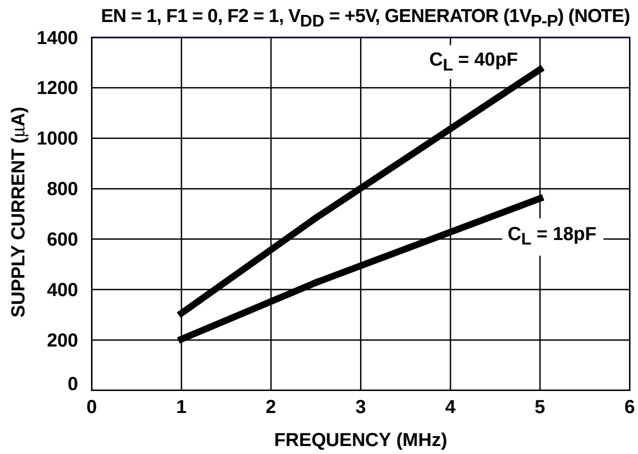



FIGURE 20. SUPPLY CURRENT vs FREQUENCY

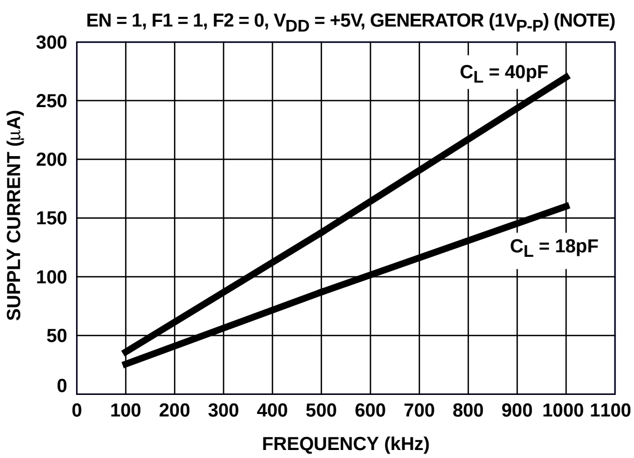



FIGURE 21. SUPPLY CURRENT vs FREQUENCY

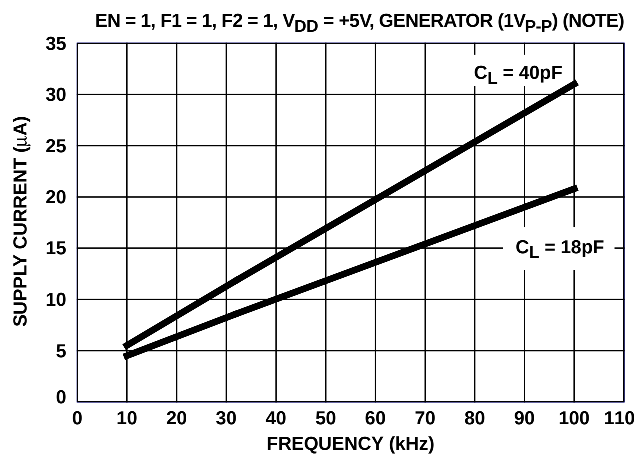



FIGURE 22. SUPPLY CURRENT vs FREQUENCY

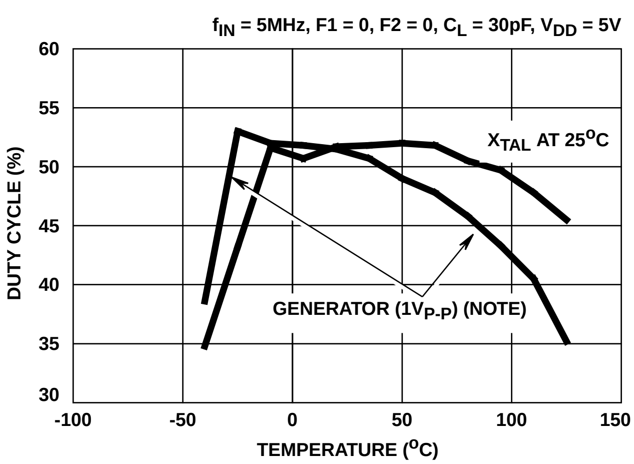



FIGURE 23. DUTY CYCLE vs TEMPERATURE

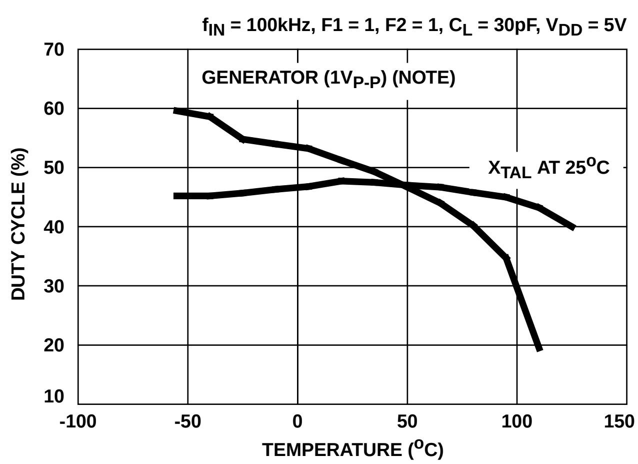



FIGURE 24. DUTY CYCLE vs TEMPERATURE

NOTE: Refer to Test Circuit (Figure 1).

## *Typical Performance Curves* (Continued)

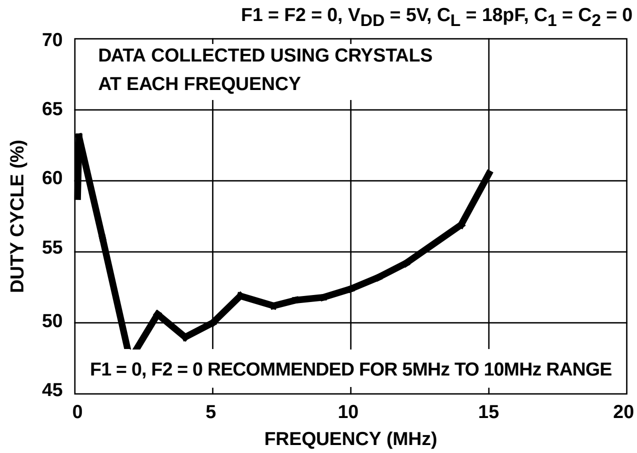



FIGURE 25. DUTY CYCLE vs FREQUENCY

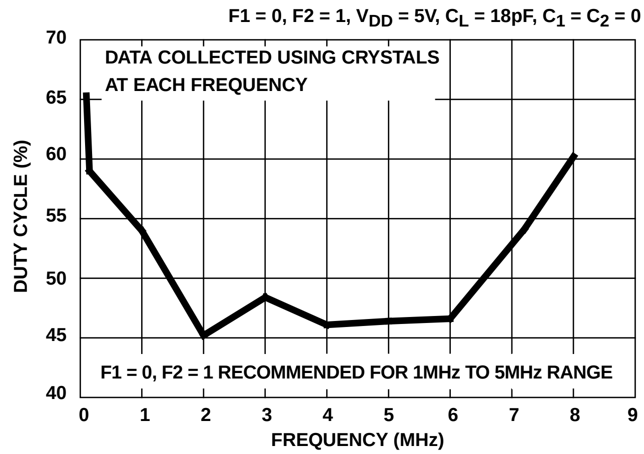



FIGURE 26. DUTY CYCLE vs FREQUENCY

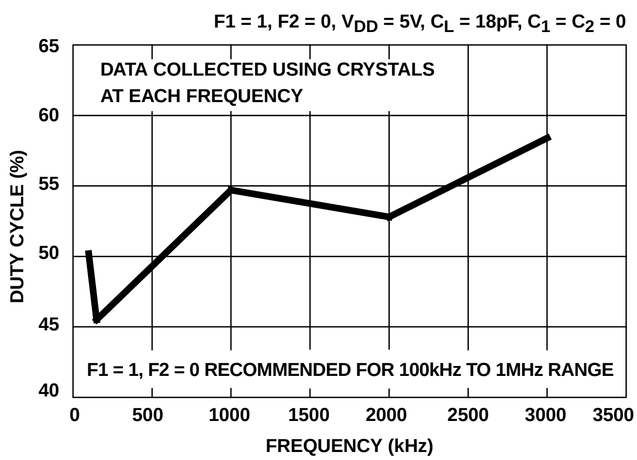



FIGURE 27. DUTY CYCLE vs FREQUENCY

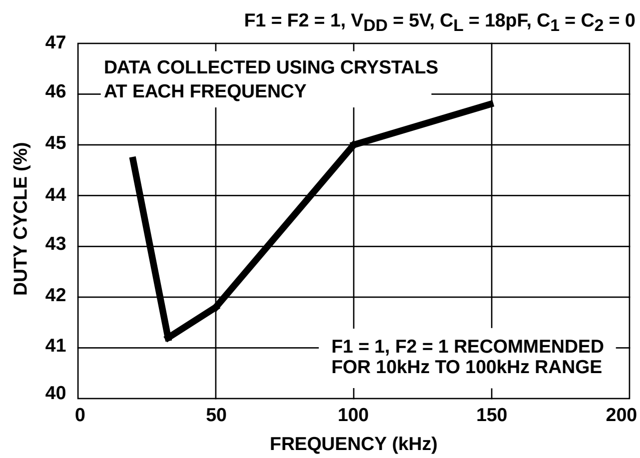



FIGURE 28. DUTY CYCLE vs FREQUENCY

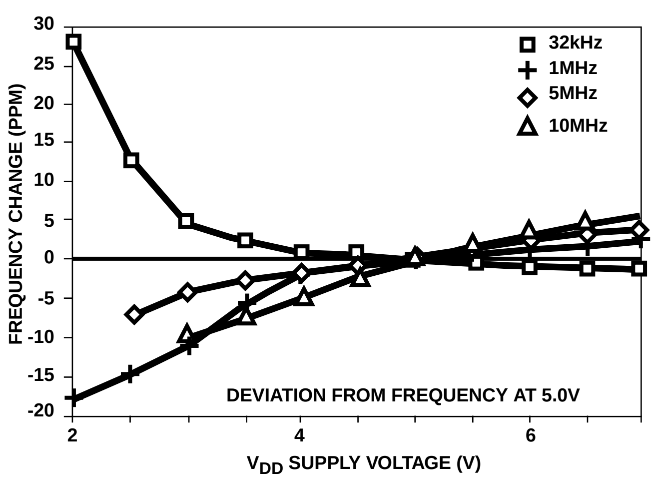



FIGURE 29. FREQUENCY CHANGE vs $V_{DD}$

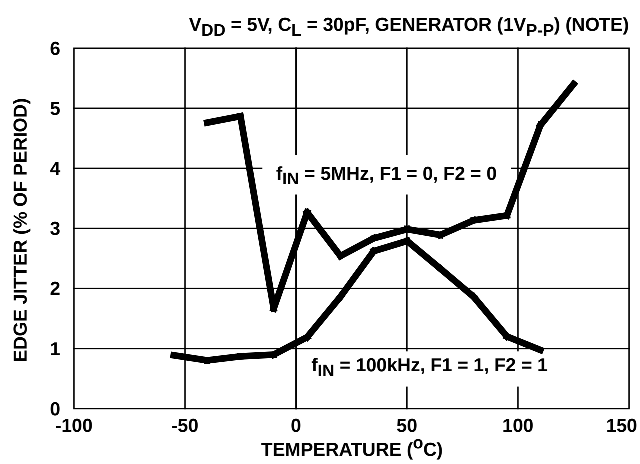



FIGURE 30. EDGE JITTER vs TEMPERATURE

NOTE: Refer to Test Circuit (Figure 1).

## *Typical Performance Curves* (Continued)

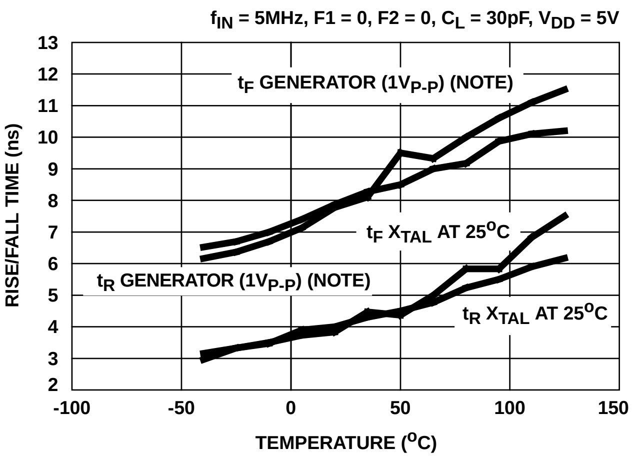



FIGURE 31. RISE/FALL TIME vs TEMPERATURE

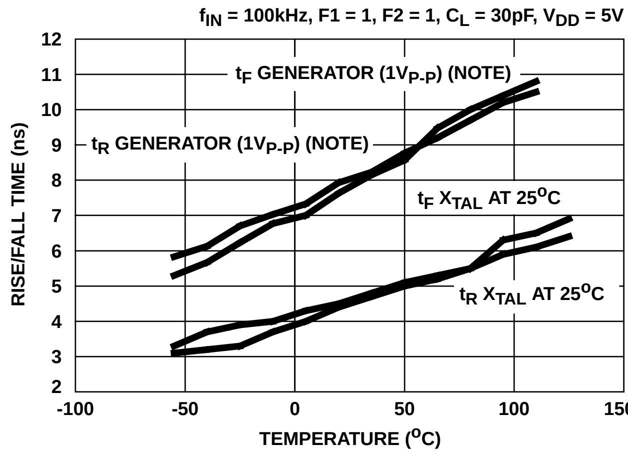



FIGURE 32. RISE/FALL TIME vs TEMPERATURE

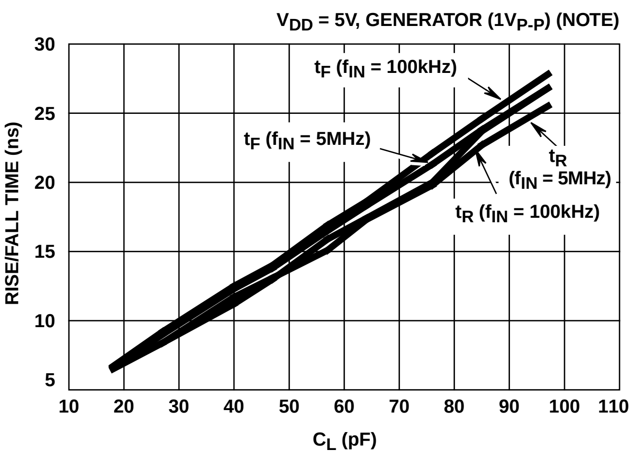



FIGURE 33. RISE/FALL TIME vs $C_L$

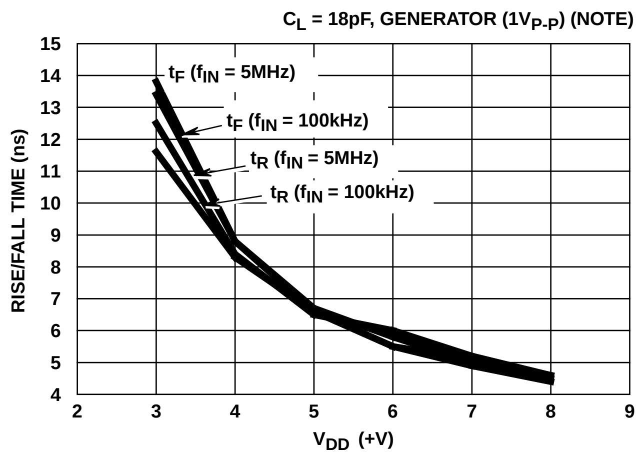



FIGURE 34. RISE/FALL TIME vs $V_{DD}$

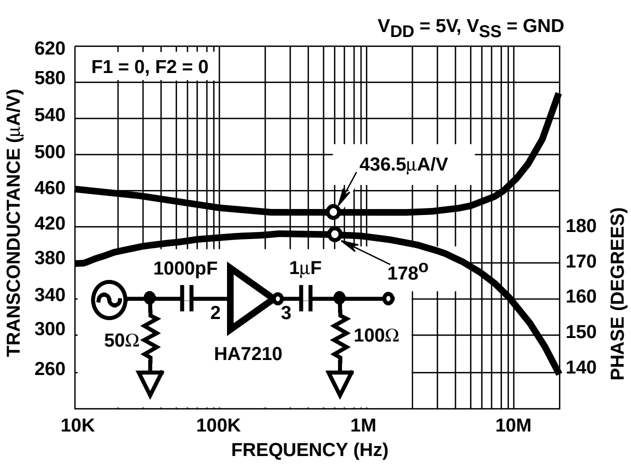



FIGURE 35. TRANSCONDUCTANCE vs FREQUENCY

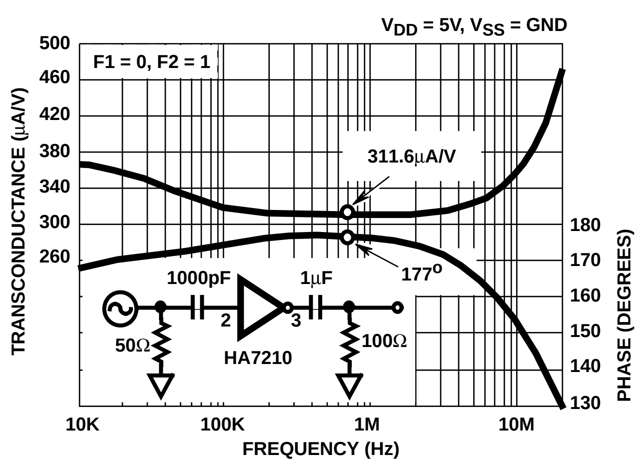



FIGURE 36. TRANSCONDUCTANCE vs FREQUENCY

NOTE: Refer to Test Circuit (Figure 1).

## *Typical Performance Curves* (Continued)

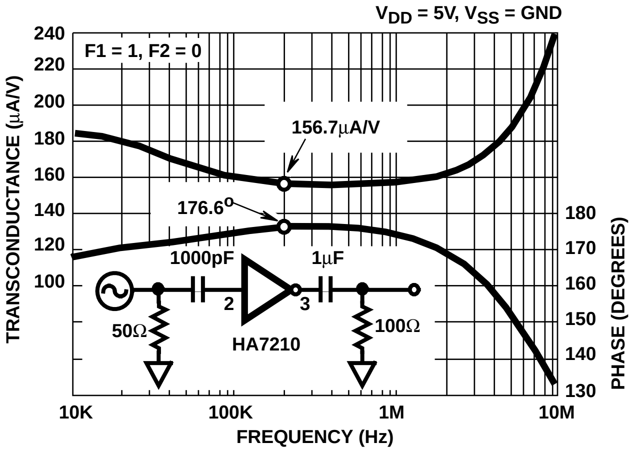



**FIGURE 37. TRANSCONDUCTANCE vs FREQUENCY**

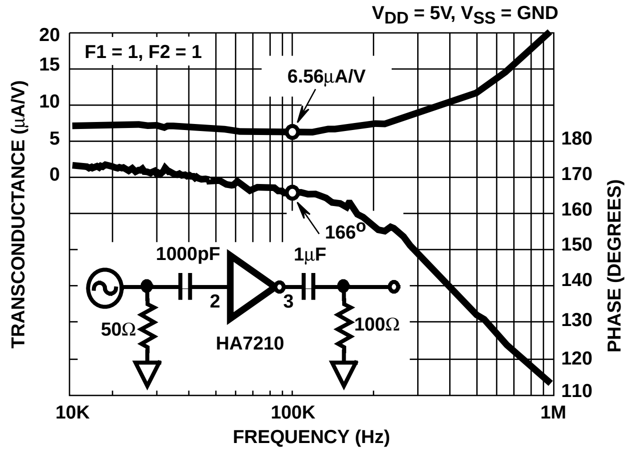
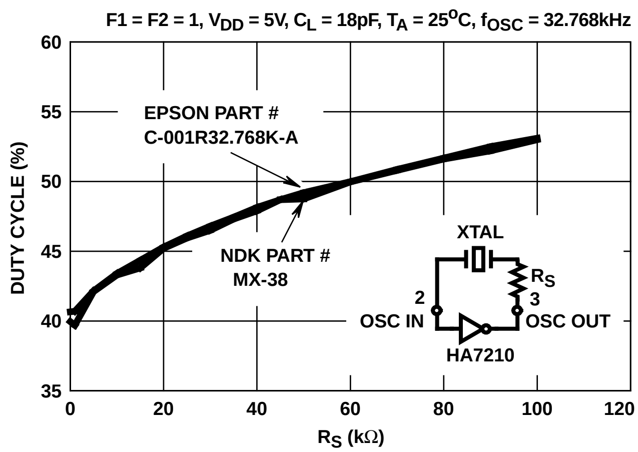



**FIGURE 38. TRANSCONDUCTANCE vs FREQUENCY**




NOTE: Figure 39 (Duty Cycle vs $R_S$ at 32kHz) should only be used for 32kHz crystals. $R_S$ may be used at other frequencies to adjust Duty Cycle but experimentation will be required to find an appropriate value. The $R_S$ value will be proportional to the effective series resistance of the crystal being used.

**FIGURE 39. DUTY CYCLE vs $R_S$ at 32kHz**

NOTE: Refer to Test Circuit (Figure 1).

## Die Characteristics

**DIE DIMENSIONS:**

68 mils x 64 mils x 14 mils

**METALLIZATION:**

Type: Si - Al
Thickness: 10kÅ ±1kÅ

**SUBSTRATE POTENTIAL**

$V_{SS}$

**PASSIVATION:**

Type: Nitride ($Si_3N_4$) Over Silox ($SiO_2$, 3% Phos)
Silox Thickness: 7kÅ ±1kÅ
Nitride Thickness: 8kÅ ±1kÅ

## Metallization Mask Layout

**HA7210**