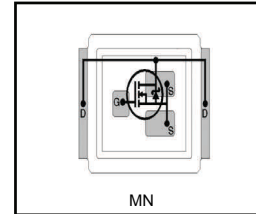


DirectFET™ Power MOSFET ②
Typical values (unless otherwise specified)

- RoHs Compliant ①
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specific MOSFETs
- Optimized for Synchronous Rectification for 5V to 12V outputs
- Low Conduction Losses
- Ideal for 24V input Primary Side Forward Converters
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①

V _{DS}		V _{GS}		R _{DS(on)}	
60V min		±20V max		5.5mΩ @ 10V	
Q _{g tot}	Q _{gd}	Q _{gs2}	Q _{rr}	Q _{oss}	V _{gs(th)}
36nC	14nC	2.7nC	37nC	11nC	4.0V



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details) ①

SH	SJ	SP		MZ	MN				
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Description

The IRF6648PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.7 mm profile. The DirectFET™ package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. Application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET™ package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6648PbF is an optimized switch for use in synchronous rectification circuits with 5-12V_{out}, and is also ideal for use as a primary side switch in 24V_{in} forward converters. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF6648TRPbF	DirectFET™ Medium Can	Tape and Reel	4800	IRF6648TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	60	V
V _{GS}	Gate-to-Source Voltage	±20	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)④	86	A
I _D @ T _C = 70°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)④	69	
I _{DM}	Pulsed Drain Current⑤	260	
E _{AS}	Single Pulse Avalanche Energy ⑥	47	mJ
I _{AR}	Avalanche Current ⑥	34	A

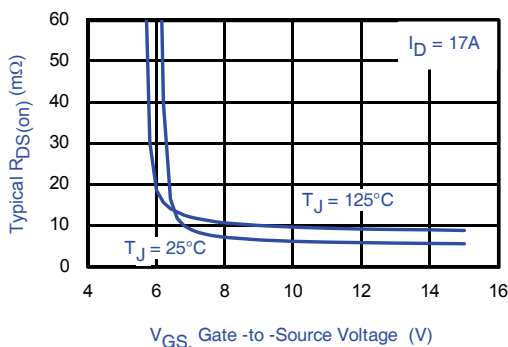


Fig 1. Typical On-Resistance vs. Gate Voltage

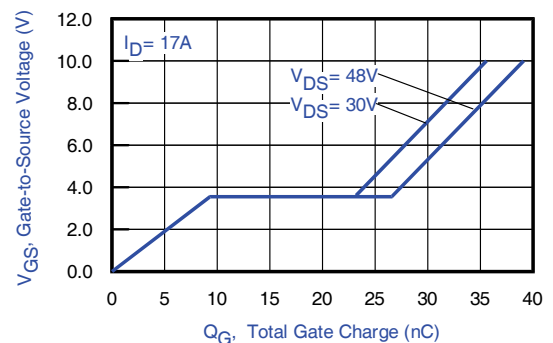


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

Notes

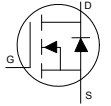
- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

- ④ TC measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting T_J = 25°C, L = 0.082mH, R_G = 25Ω, I_{AS} = 34A.

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA	
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.076	—	V/°C	Reference to 25°C, I _D = 1mA	
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	5.5	7.0	mΩ	V _{GS} = 10V, I _D = 17A	
V _{GS(th)}	Gate Threshold Voltage	3.0	4.0	4.9	V	V _{DS} = V _{GS} , I _D = 150μA	
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	—	-11	—	mV/°C		
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 60 V, V _{GS} = 0V	
		—	—	250		V _{DS} = 48 V, V _{GS} = 0V, T _J = 125°C	
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V	
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V	
g _{fs}	Forward Transconductance	31	—	—	S	V _{DS} = 10V, I _D = 17A	
Q _g	Total Gate Charge	—	36	50	nC	V _{DS} = 30V V _{GS} = 10V I _D = 17A See Fig 15	
Q _{gs1}	Pre- V _{th} Gate-to-Source Charge	—	7.5	—			
Q _{gs2}	Post- V _{th} Gate-to-Source Charge	—	2.7	—			
Q _{gd}	Gate-to-Drain Charge	—	14	21			
Q _{godr}	Gate Charge Overdrive	—	12	—			
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	17	—			
Q _{oss}	Output Charge	—	21	—			nC
R _{G(Internal)}	Gate Resistance	—	1.0	—	Ω		
t _{d(on)}	Turn-On Delay Time	—	16	—	ns	V _{DD} = 30V, V _{GS} = 10V ^⑦ I _D = 17A R _G = 6.2Ω See Fig 16 & 17	
t _r	Rise Time	—	29	—			
t _{d(off)}	Turn-Off Delay Time	—	28	—			
t _f	Fall Time	—	13	—			
C _{iss}	Input Capacitance	—	2120	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz	
C _{oss}	Output Capacitance	—	600	—			
C _{rss}	Reverse Transfer Capacitance	—	170	—			
C _{oss}	Output Capacitance		2450				V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance		440				V _{GS} = 0V, V _{DS} = 48V, f = 1.0MHz

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	81	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^⑤	—	—	260		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 17A, V _{GS} = 0V ^⑦
t _{rr}	Reverse Recovery Time	—	31	47	ns	T _J = 25°C, I _F = 17A, V _{DD} = 30V
Q _{rr}	Reverse Recovery Charge	—	37	56	nC	di/dt = 100A/μs ^⑦ See Fig. 18

Notes:

- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑦ Pulse width ≤ 400μs; duty cycle ≤ 2%.

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③④	2.8	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③④	1.8	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	89	
T_P	Peak Soldering Temperature	270	$^\circ\text{C}$
T_J	Operating Junction and	-40 to + 150	
T_{STG}	Storage Temperature Range		

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	45	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ⑧	12.5	—	
$R_{\theta JC}$	Junction-to-Can ④⑩	—	1.4	
$R_{\theta JA-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.022		$\text{W}/^\circ\text{C}$

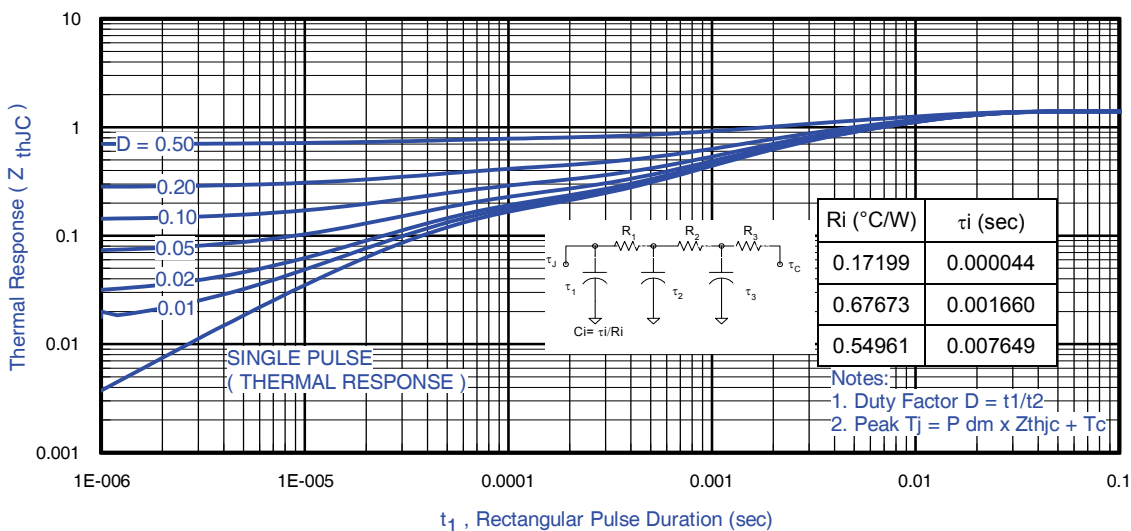


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Case

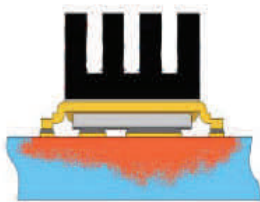
Notes:

- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④ T_C measured with thermocouple incontact with top (Drain) of part.

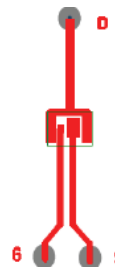
- ⑧ Used double sided cooling, mounting pad with large heatsink.
- ⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑩ R_{θ} is measured at T_J of approximately 90°C .



③ Surface mounted on 1 in. square Cu board (still air).



⑨ Mounted to a PCB with small clip heatsink (still air)



⑧ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

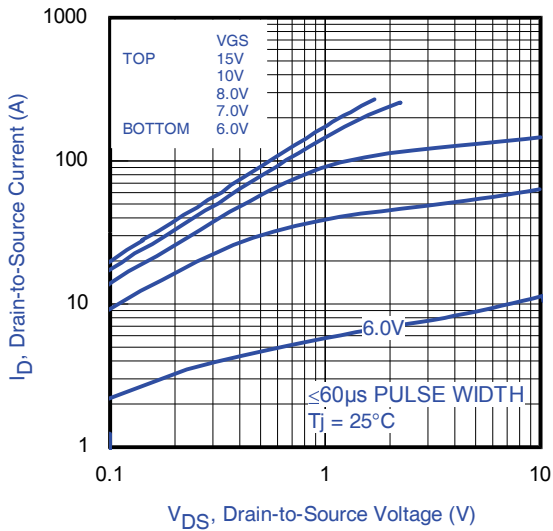


Fig 4. Typical Output Characteristics

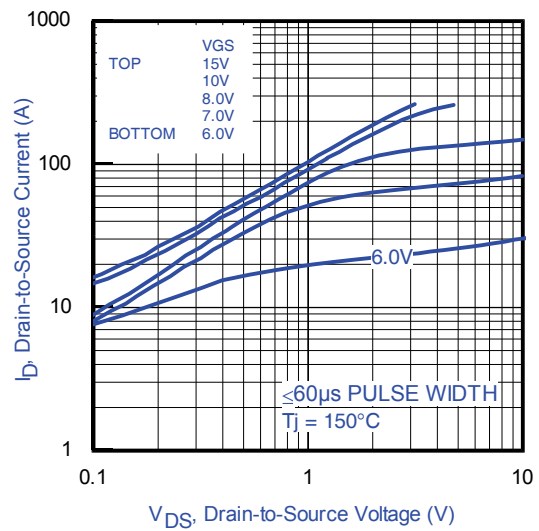


Fig 5. Typical Output Characteristics

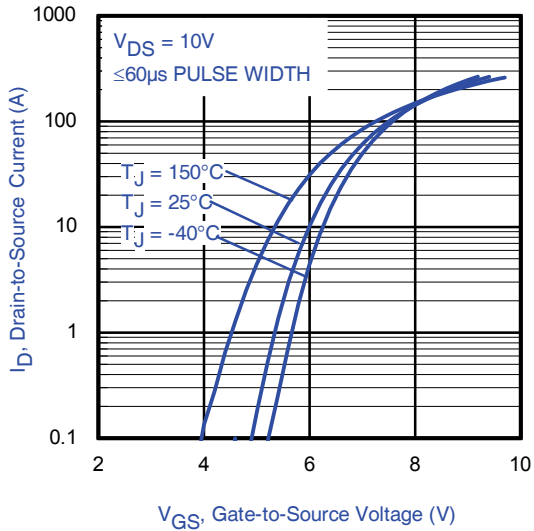


Fig 6. Typical Transfer Characteristics

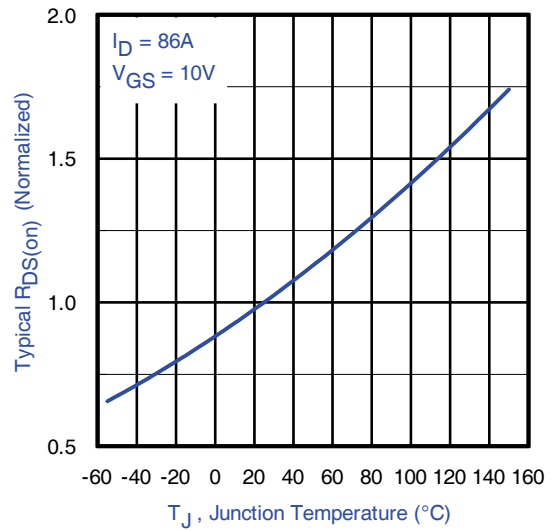


Fig 7. Normalized On-Resistance vs. Temperature

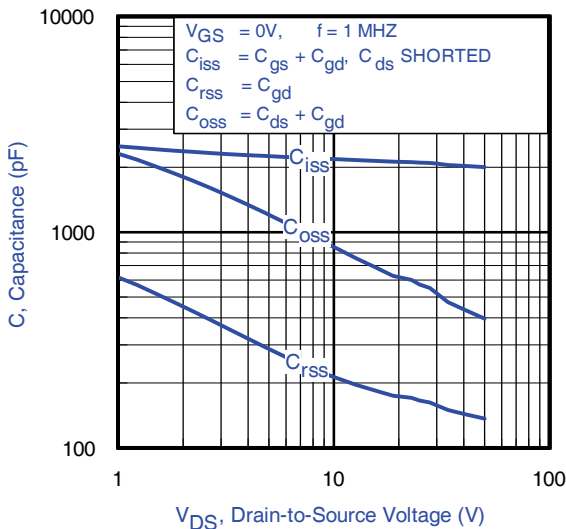


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

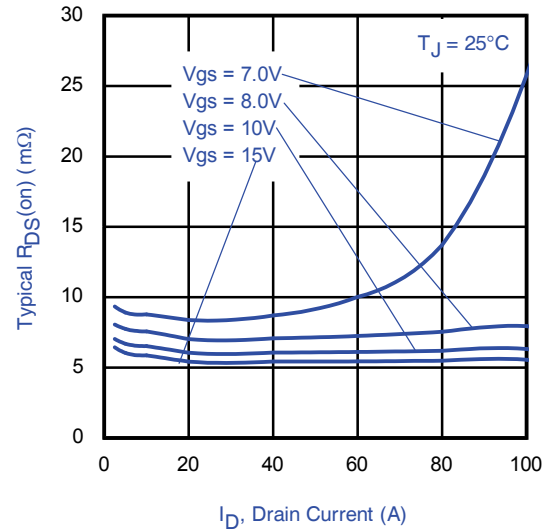


Fig 9. Normalized Typical On-Resistance vs. Drain Current and Gate Voltage

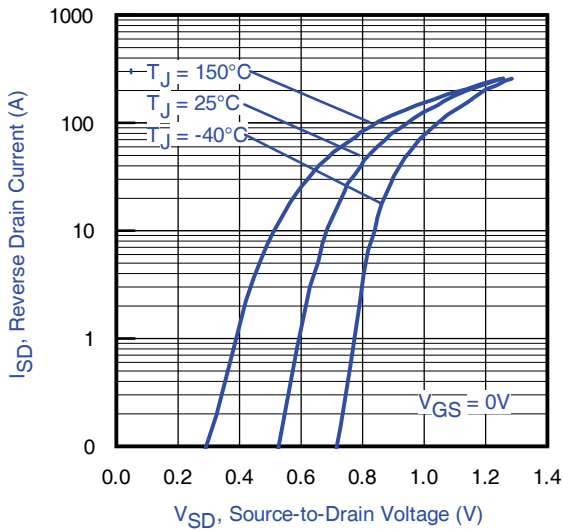


Fig 10. Typical Source-Drain Diode Forward Voltage

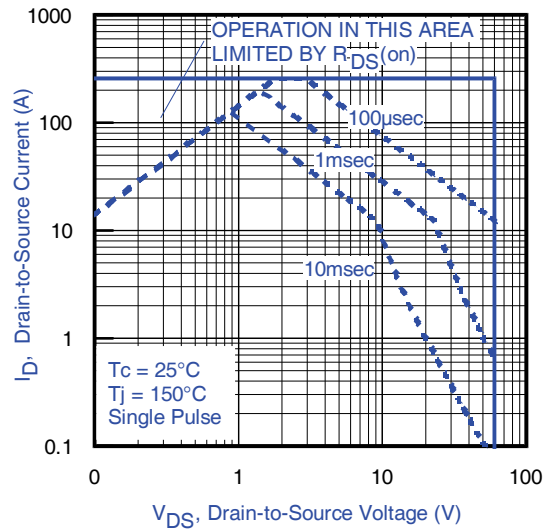


Fig 11. Maximum Safe Operating Area

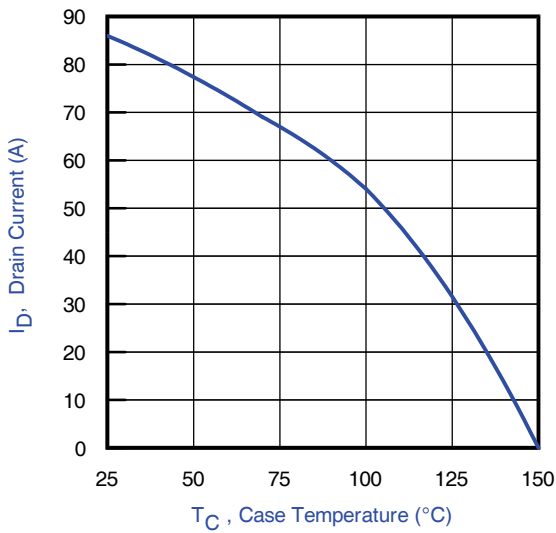


Fig 12. Maximum Drain Current vs. Case Temperature

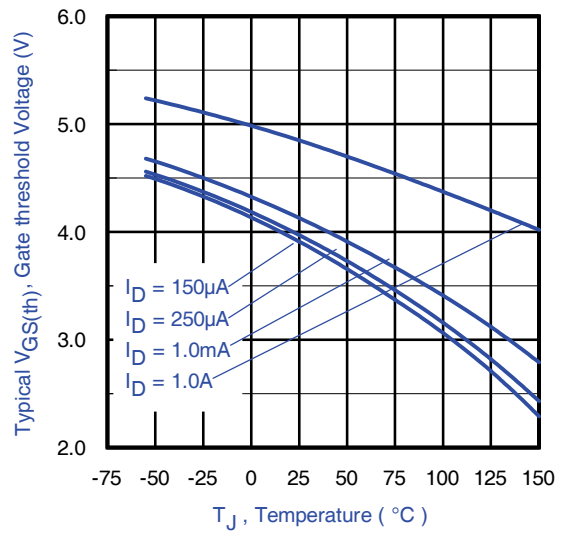


Fig 13. Typical Threshold Voltage vs. Junction Temperature

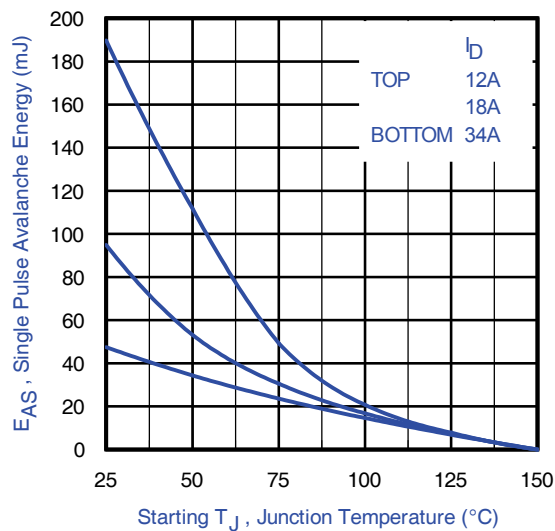


Fig 14. Maximum Avalanche Energy vs. Drain Current

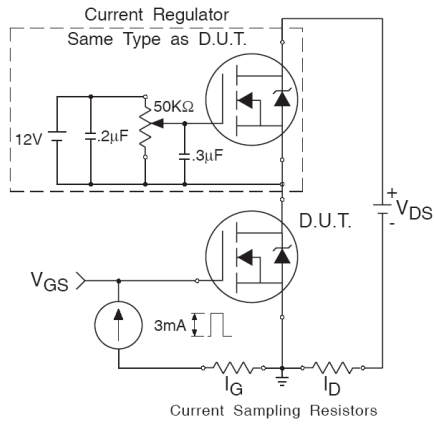


Fig 15a. Gate Charge Test Circuit

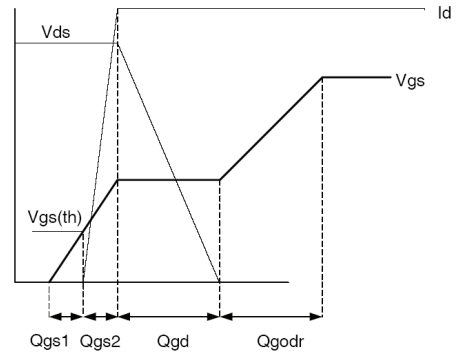


Fig 15b. Gate Charge Waveform

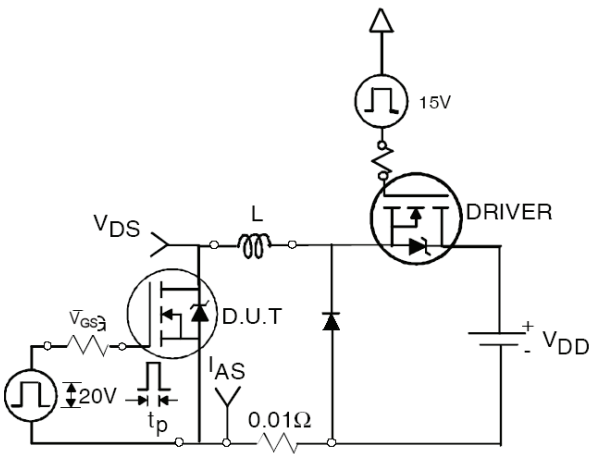


Fig 16a. Unclamped Inductive Test Circuit

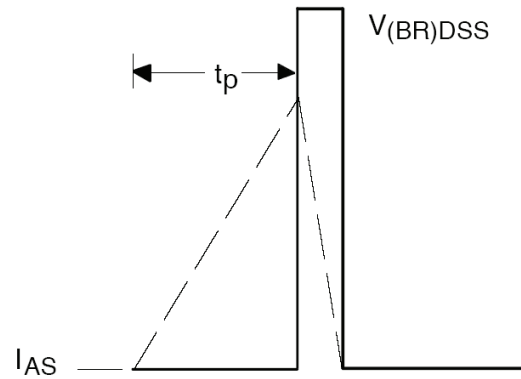


Fig 16b. Unclamped Inductive Waveforms

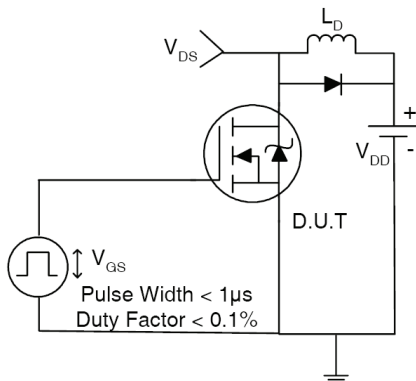


Fig 17a. Switching Time Test Circuit

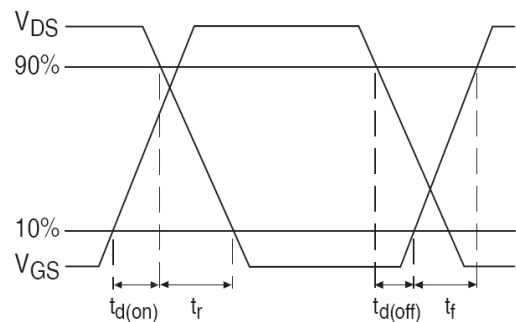


Fig 17b. Switching Time Waveforms

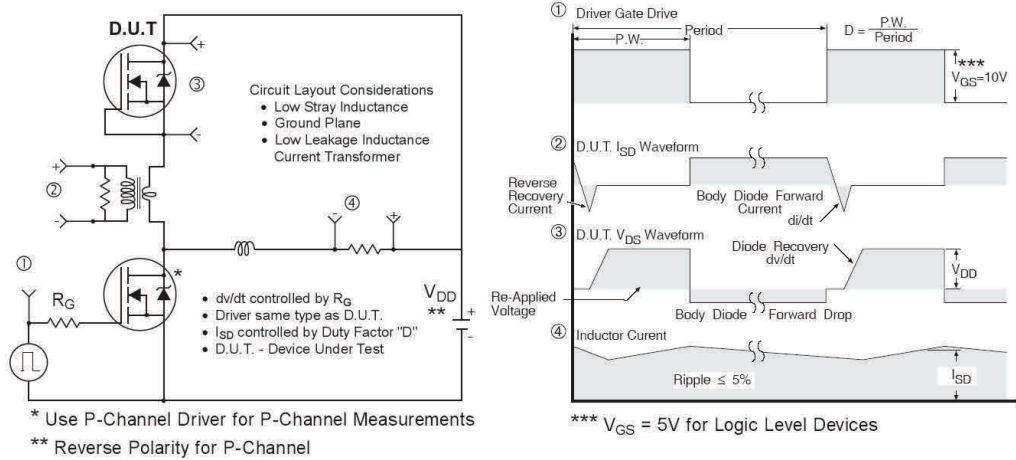
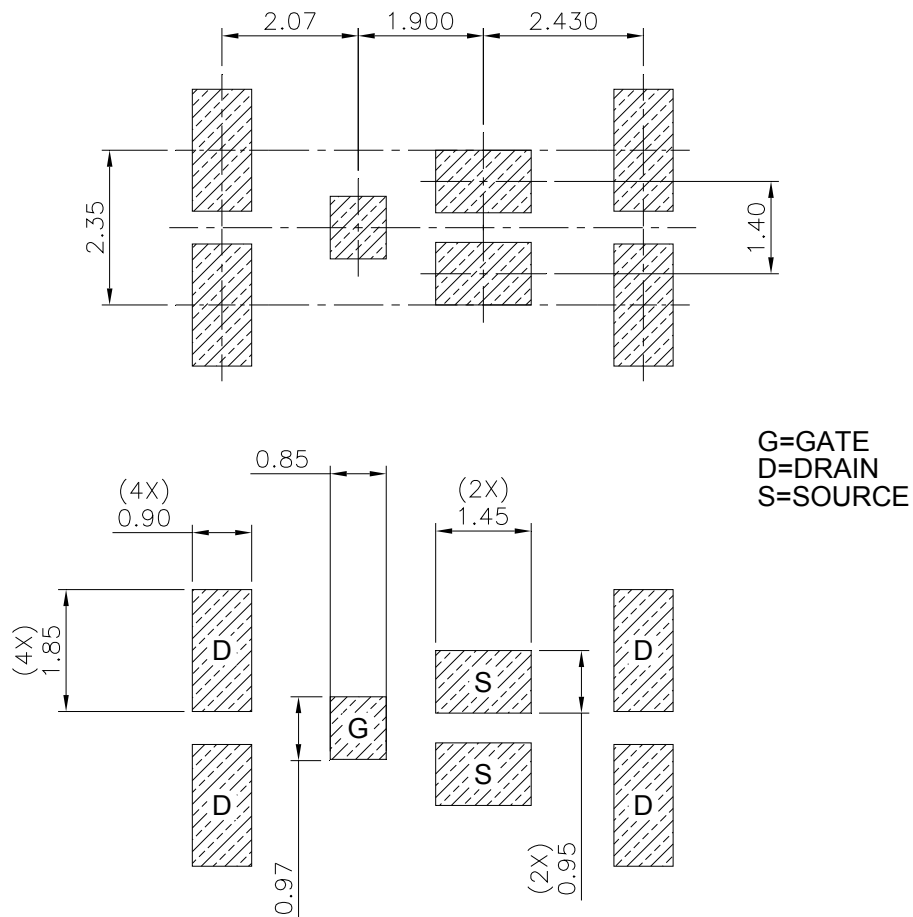


Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

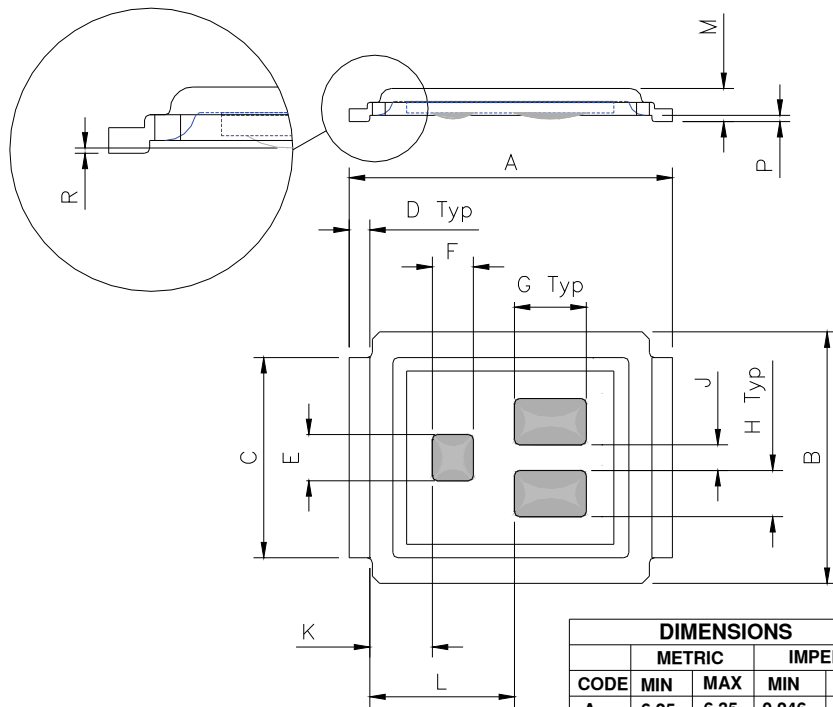
DirectFET™ Substrate and PCB Layout, MN Outline ③ (Medium Size Can, N-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



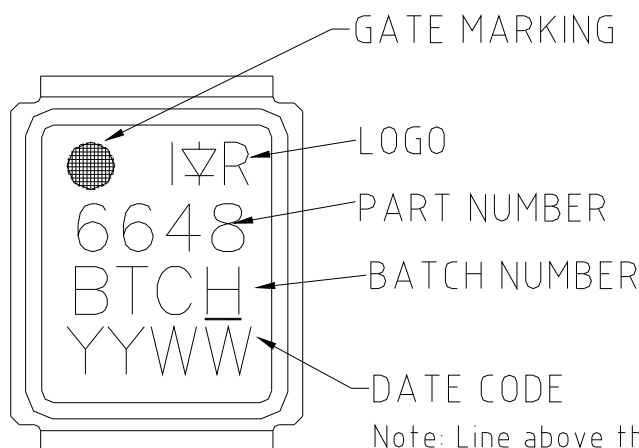
**DirectFET™ Outline Dimension, MN Outline
(Medium Size Can, N-Designation).**

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



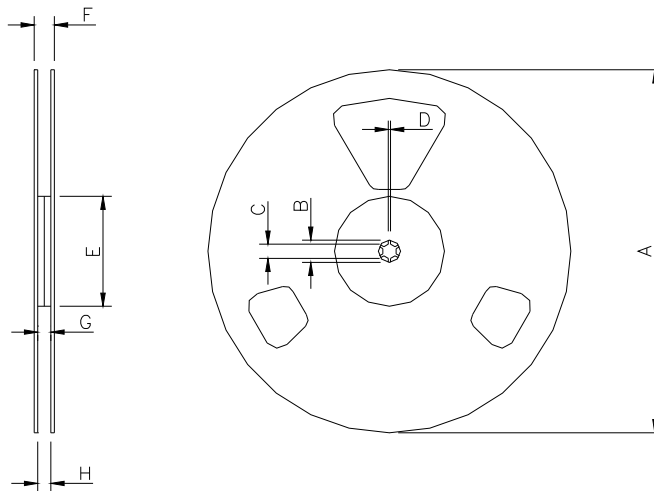
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.201
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.88	0.92	0.034	0.036
F	0.78	0.82	0.031	0.032
G	1.38	1.42	0.054	0.056
H	0.88	0.92	0.034	0.036
J	0.48	0.52	0.019	0.020
K	1.16	1.29	0.046	0.051
L	2.74	2.91	0.109	0.115
M	0.616	0.676	0.0235	0.0274
R	0.020	0.080	0.0008	0.0031
P	0.08	0.17	0.003	0.007

DirectFET™ Part Marking



Note: Line above the last character of the date-code indicates "Lead-Free".

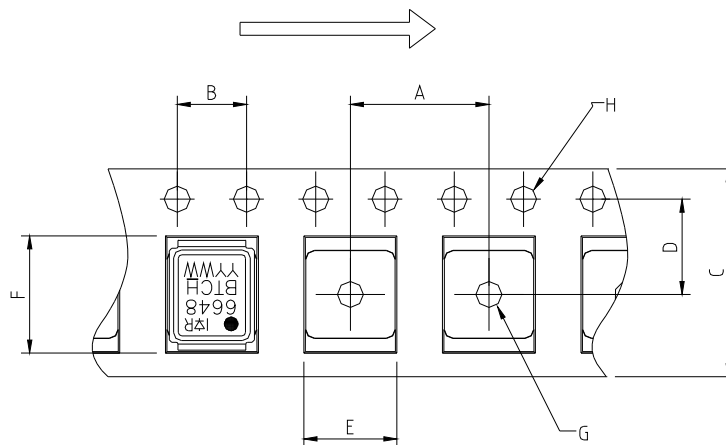
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
 Std reel quantity is 4800 parts. (ordered as IRF6648TRPbF). For 1000 parts on 7" reel, order IRF6648TR1PbF

REEL DIMENSIONS								
CODE	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

LOADED TAPE FEED DIRECTION



DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Qualification Information

Qualification Level	Consumer [†]	
Moisture Sensitivity Level	DirectFET [®] Medium Can	MSL1 (per JEDEC J-STD-020D [†])
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
04/06/2017	<ul style="list-style-type: none"> • Changed datasheet with Infineon logo - all pages. • Added Orderable table on page 1. • Corrected PCB layout on page 7 • Added Qualification table on page 10. • Added disclaimer on last page.

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