HV5308 / HV5408

32-Channel, Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs

Features

- Processed with High-Voltage CMOS technology
- Low power-level shifting
- Source/sink current minimum 20mA
- Shift register speed 8.0 MHz
- Latched data outputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Diode to V_{PP} allows efficient power recovery

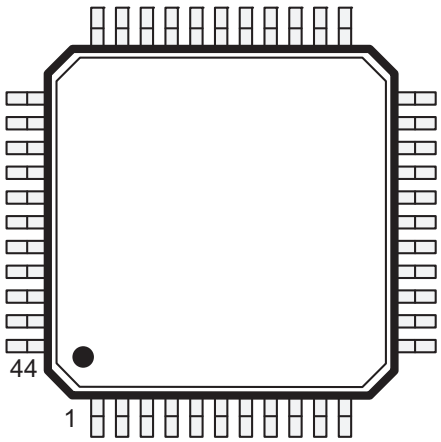
Description

HV5308 and HV5408 are low-voltage serial to high-voltage parallel converters with push-pull outputs. These devices have been designed for use as a driver for AC-electroluminescent displays. HV5308 / HV5408 can also be used in any application requiring multiple output high-voltage, current sourcing, and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

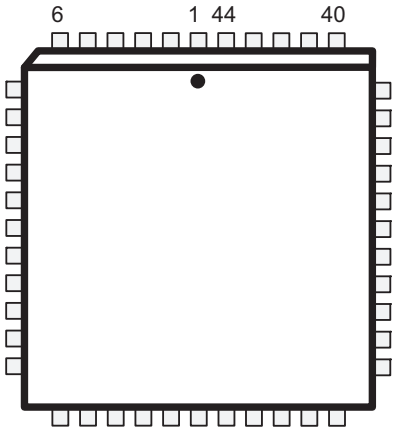
These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. Data is shifted through the shift register on the low-to-high transition of the clock. HV5308 shifts in the clockwise direction, when viewed from the top of the package, and HV5408 shifts in the counter-clockwise direction.

A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ input is high. The data in the latch is retained when $\overline{LE}$ is low.

Package Type



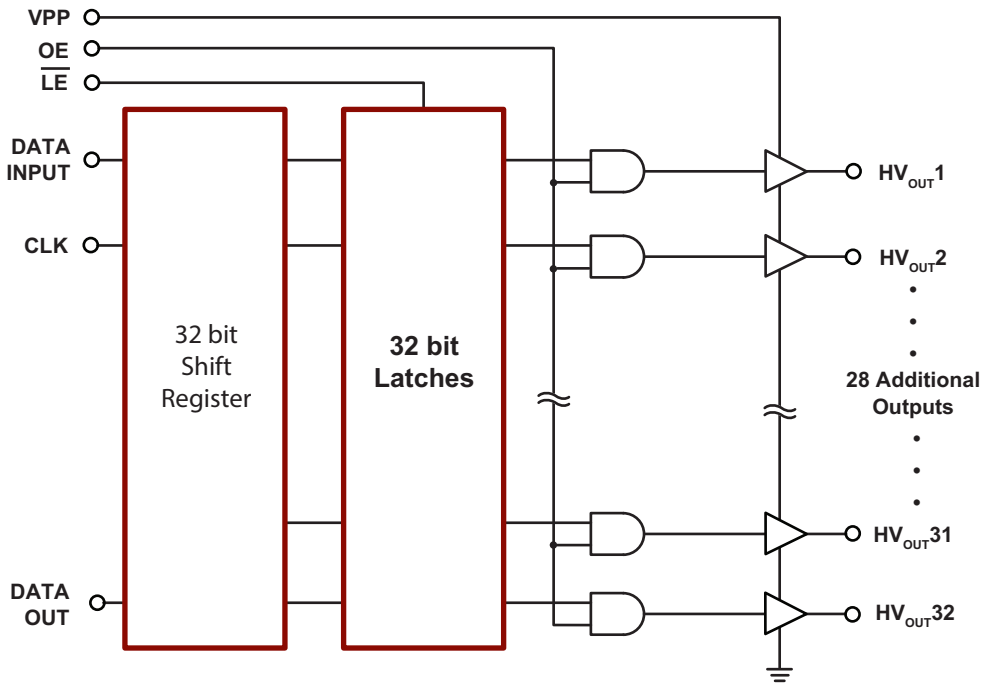
44-Lead PQFP



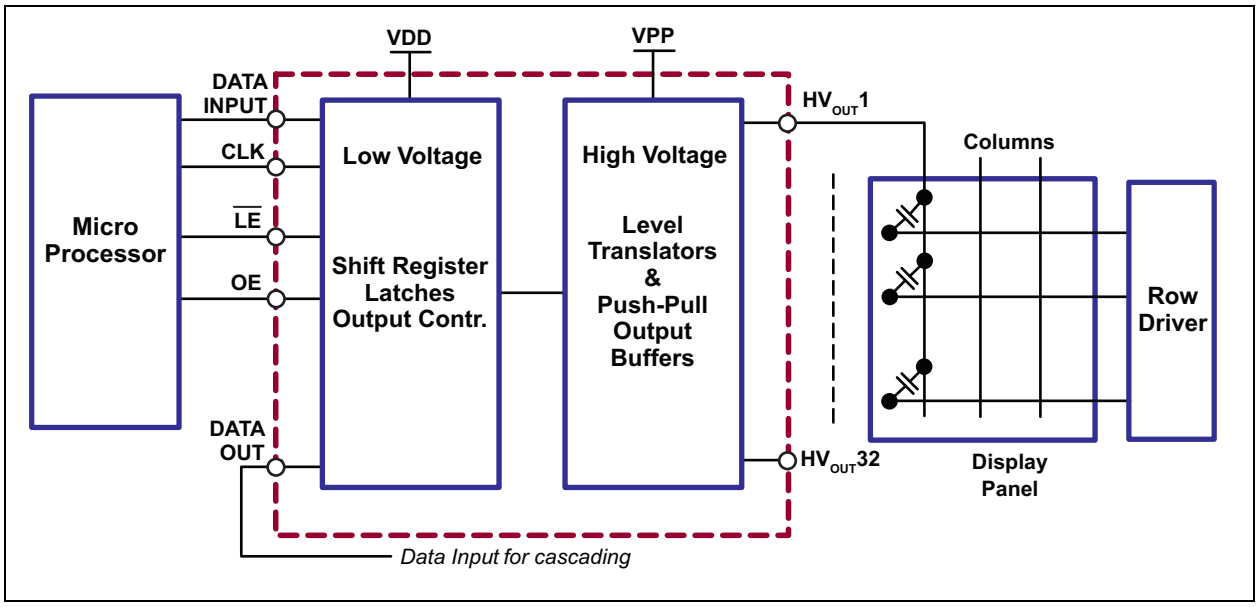
44-Lead PLCC

See Table 2-1 for pin information

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Supply voltage, V_{DD} ..... -0.5V to +16V
Supply voltage, V_{PP} ..... -0.5V to +90V
Logic input levels ..... -0.5V to V_{DD}+0.5V
Ground current[1] 1.5A
Continuous total power dissipation[2] 1200mW
Operating temperature range ..... -40°C to +85°C
Storage temperature range ..... -65°C to +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1: Duty cycle is limited by the total power dissipated in the package.

2: For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{PP} = 60V, V_{DD} = 12V, T_A = 25°C

Parameter		Symbol	Min	Max	Units	Conditions
DC Characteristics						
V_{PP} supply current		I_{PP}	-	0.5	mA	$HV_{OUTPUTS}$ high to low
I_{DD} supply current (quiescent)		I_{DDQ}	-	100	µA	All inputs = V_{DD} or GND
I_{DD} supply current (operating)		I_{DD}	-	15	mA	V_{DD}= V_{DD} max, f_{CLK}= 8.0MHz
High level logic input current		I_{IH}	-	1.0	µA	V_{IN}= V_{DD}
Low level logic input current		I_{IL}	-	-1.0	µA	V_{IN}= 0
High level output voltage	HV_{OUT}	V_{OH}	52	-	V	I_{OH}= -20mA, -40 to 85°C I_{OH}= -15mA, -55 to 125°C
	Data out		10.5	-	V	I_O= -100µA
Low level output voltage	HV_{OUT}	V_{OL}	-	8.0	V	I_{OL}= 20mA, -40 to 85°C I_{OL}= 15mA, -55 to 125°C
	Data out		-	1.0	V	I_O= 100µA
HV output clamp diode voltage		V_{OC}	-	-1.5	V	I_{OL}= -100mA
AC Characteristics						
Clock frequency		f_{CLK}	-	8.0	MHz	---
Clock width, High or Low		t_{WL} or t_{WH}	62	-	ns	---
Setup time before CLK rises		t_{SU}	25	-	ns	---
Hold time after CLK rises		t_H	10	-	ns	---
Data output delay after L to H CLK		t_{DLH} (Data)	-	110	ns	C_L= 15pF, (**Note 1**)
Data output delay after H to L CLK		t_{DHL} (Data)	-	110	ns	C_L= 15pF, (**Note 1**)
$\overline{LE}$ delay after L to H CLK		t_{DLE}	50	-	ns	(**Note 1**)
Width of $\overline{LE}$ pulse		t_{WLE}	50	-	ns	---
$\overline{LE}$ setup time before L to H CLK		t_{SLE}	50	-	ns	(**Note 1**)
Delay from $\overline{LE}$ to HV_{OUT}, L to H		t_{ON}	-	500	ns	(**Note 1**)
Delay from $\overline{LE}$ to HV_{OUT}, H to L		t_{OFF}	-	500	ns	(**Note 1**)

Note 1: L to H = Low to High; H to L = High to Low.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J$ = +25°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature		-40	–	85	°C	
Storage Temperature		-65	–	150	°C	
Package Thermal Resistances						
Thermal Resistance, 44-Lead PQFP	θ_{ja}	–	51	–	°C/W	
Thermal Resistance, 44-Lead PLCC	θ_{ja}	–	37	–	°C/W	

2.0 PIN DESCRIPTION

The locations of the pins are listed in Package Type.

TABLE 2-1: PIN DESCRIPTION PQFP

Pin #	HV5308	HV5408	Description
1	$HV_{OUT}22$	$HV_{OUT}11$	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to V_{PP} rail levels.
2	$HV_{OUT}21$	$HV_{OUT}12$	
3	$HV_{OUT}20$	$HV_{OUT}13$	
4	$HV_{OUT}19$	$HV_{OUT}14$	
5	$HV_{OUT}18$	$HV_{OUT}15$	
6	$HV_{OUT}17$	$HV_{OUT}16$	
7	$HV_{OUT}16$	$HV_{OUT}17$	
8	$HV_{OUT}15$	$HV_{OUT}18$	
9	$HV_{OUT}14$	$HV_{OUT}19$	
10	$HV_{OUT}13$	$HV_{OUT}20$	
11	$HV_{OUT}12$	$HV_{OUT}21$	
12	$HV_{OUT}11$	$HV_{OUT}22$	
13	$HV_{OUT}10$	$HV_{OUT}23$	
14	$HV_{OUT}9$	$HV_{OUT}24$	
15	$HV_{OUT}8$	$HV_{OUT}25$	
16	$HV_{OUT}7$	$HV_{OUT}26$	
17	$HV_{OUT}6$	$HV_{OUT}27$	
18	$HV_{OUT}5$	$HV_{OUT}28$	
19	$HV_{OUT}4$	$HV_{OUT}29$	
20	$HV_{OUT}3$	$HV_{OUT}30$	
21	$HV_{OUT}2$	$HV_{OUT}31$	
22	$HV_{OUT}1$	$HV_{OUT}32$	
23	DATA OUT	DATA OUT	Serial data output. Data output for cascading to the data input of the next device.
24	N/C	N/C	No connect.
25			
26			
27	CLK	CLK	Data shift register clock Input are shifted into the shift register on the positive edge of the clock.
28	GND	GND	Logic and high voltage ground
29	VPP	VPP	High voltage power rail.
30	VDD	VDD	Low voltage logic power rail.
31	$\overline{LE}$	$\overline{LE}$	Latch enable input. When $\overline{LE}$ is High, shift register data is transferred into a data latch. When $\overline{LE}$ is Low, data is latched, and new data can be clocked into the shift register.
32	DATA IN	DATA IN	Serial data input. Data needs to be present before each rising edge of the clock.
33	OE	OE	Output enable input. When OE is Low, all HV outputs are forced into a Low state, regardless of data in each channel. When OE is High, all HV outputs reflect data latched.
34	N/C	N/C	No connect.

TABLE 2-1: PIN DESCRIPTION PQFP (CONTINUED)

Pin #	HV5308	HV5408	Description
35	$HV_{OUT}32$	$HV_{OUT}1$	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to V_{PP} rail levels.
36	$HV_{OUT}31$	$HV_{OUT}2$	
37	$HV_{OUT}30$	$HV_{OUT}3$	
38	$HV_{OUT}29$	$HV_{OUT}4$	
39	$HV_{OUT}28$	$HV_{OUT}5$	
40	$HV_{OUT}27$	$HV_{OUT}6$	
41	$HV_{OUT}26$	$HV_{OUT}7$	
42	$HV_{OUT}25$	$HV_{OUT}8$	
43	$HV_{OUT}24$	$HV_{OUT}9$	
44	$HV_{OUT}23$	$HV_{OUT}10$	

TABLE 2-2: PIN DESCRIPTION PLCC

Pin #	HV5308	HV5408	Description
1	$HV_{OUT}17$	$HV_{OUT}16$	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to V_{PP} rail levels.
2	$HV_{OUT}16$	$HV_{OUT}17$	
3	$HV_{OUT}15$	$HV_{OUT}18$	
4	$HV_{OUT}14$	$HV_{OUT}19$	
5	$HV_{OUT}13$	$HV_{OUT}20$	
6	$HV_{OUT}12$	$HV_{OUT}21$	
7	$HV_{OUT}11$	$HV_{OUT}22$	
8	$HV_{OUT}10$	$HV_{OUT}23$	
9	$HV_{OUT}9$	$HV_{OUT}24$	
10	$HV_{OUT}8$	$HV_{OUT}25$	
11	$HV_{OUT}7$	$HV_{OUT}26$	
12	$HV_{OUT}6$	$HV_{OUT}27$	
13	$HV_{OUT}5$	$HV_{OUT}28$	
14	$HV_{OUT}4$	$HV_{OUT}29$	
15	$HV_{OUT}3$	$HV_{OUT}30$	
16	$HV_{OUT}2$	$HV_{OUT}31$	
17	$HV_{OUT}1$	$HV_{OUT}32$	
18	DATA OUT	DATA OUT	Serial data output. Data output for cascading to the data input of the next device.
19	N/C	N/C	No connect.
20			
21			
22	CLK	CLK	Data shift register clock Input are shifted into the shift register on the positive edge of the clock.
23	GND	GND	Logic and high voltage ground
24	VPP	VPP	High voltage power rail.
25	VDD	VDD	Low voltage logic power rail.
26	LE	LE	Latch enable input. When $\overline{LE}$ is High, shift register data is transferred into a data latch. When $\overline{LE}$ is Low, data is latched, and new data can be clocked into the shift register.

TABLE 2-2: PIN DESCRIPTION PLCC (CONTINUED)

Pin #	HV5308	HV5408	Description
27	DATA IN	DATA IN	Serial data input. Data needs to be present before each rising edge of the clock.
28	OE	OE	Output enable input. When OE is Low, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is High, all HV outputs reflect data latched.
29	N/C	N/C	No connect.
30	HVOUT32	$HV_{OUT}1$	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to V_{PP} rail levels.
31	HVOUT31	$HV_{OUT}2$	
32	HVOUT30	$HV_{OUT}3$	
33	HVOUT29	$HV_{OUT}4$	
34	HVOUT28	$HV_{OUT}5$	
35	HVOUT27	$HV_{OUT}6$	
36	HVOUT26	$HV_{OUT}7$	
37	HVOUT25	$HV_{OUT}8$	
38	HVOUT24	$HV_{OUT}9$	
39	HVOUT23	$HV_{OUT}10$	
40	HVOUT22	$HV_{OUT}11$	
41	HVOUT21	$HV_{OUT}12$	
42	HVOUT20	$HV_{OUT}13$	
43	HVOUT19	$HV_{OUT}14$	
44	HVOUT18	$HV_{OUT}15$	

3.0 FUNCTIONAL DESCRIPTION

Table 3-1 provides functional information about HV5308 / HV5408.

TABLE 3-1: FUNCTIONAL TABLE CLK

DATA IN	CLK	DATA OUT
H	↑	H
L	↑	L
X	No ↑	No change

Note: H = High level, L = Low level, ↑ = Low-to-High transition

TABLE 3-2: FUNCTIONAL TABLE $\overline{LE}$, OE

DATA IN	$\overline{LE}$	OE	HV_{OUT}
X	X	L	All HV_{OUT}= Low
X	L	H	Previous latched data
H	H	H	H
L	H	H	L

Note: H = High level, L = Low level, X= Don't Care

3.1 Power-Up and Recommended Operating Conditions

To power-up HV5308 / HV5408, perform the following power-up sequence:

1. Connect ground
2. Apply V_{DD}
3. Set all inputs (Data, CLK, $\overline{LE}$, etc.) to a known state
4. Apply V_{PP}
5. The V_{PP} should not fall below V_{DD} or float during operation.

To power-down the device, reverse the steps above.

TABLE 3-3: RECOMMENDED OPERATING CONDITIONS (-40°C to 85°C)

Symbol	Parameter	Min	Max	Units
V_{DD}	Logic voltage supply	10.8	13.2	V
V_{PP}	High voltage supply	8.0	80	V
V_{IH}	Input high voltage	V_{DD}- 2.0	V_{DD}	V
V_{IL}	Input low voltage	0	2.0	V
f_{CLK}	Clock frequency	0	8.0	MHz

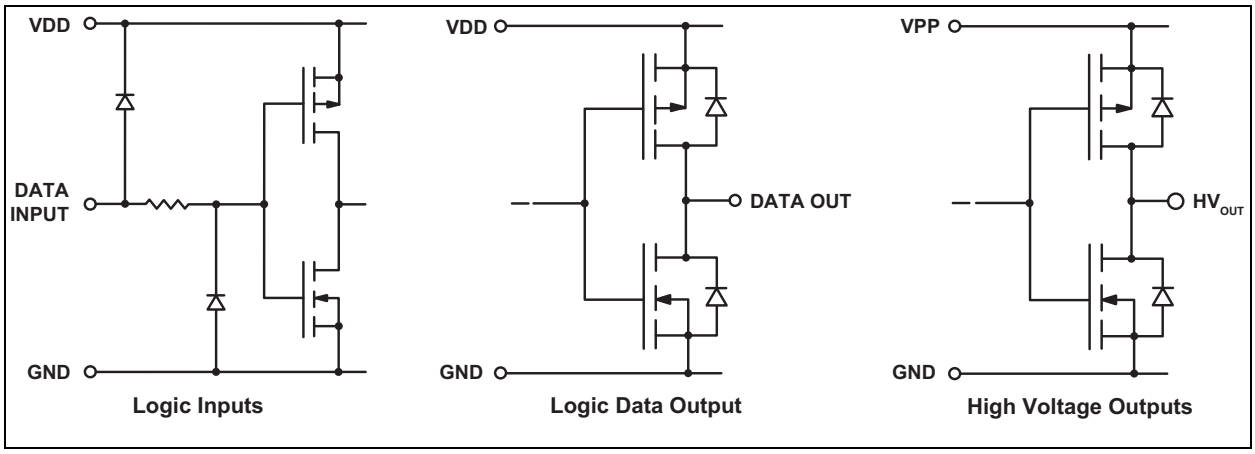


FIGURE 3-1: *Input and Output Equivalent Circuits*

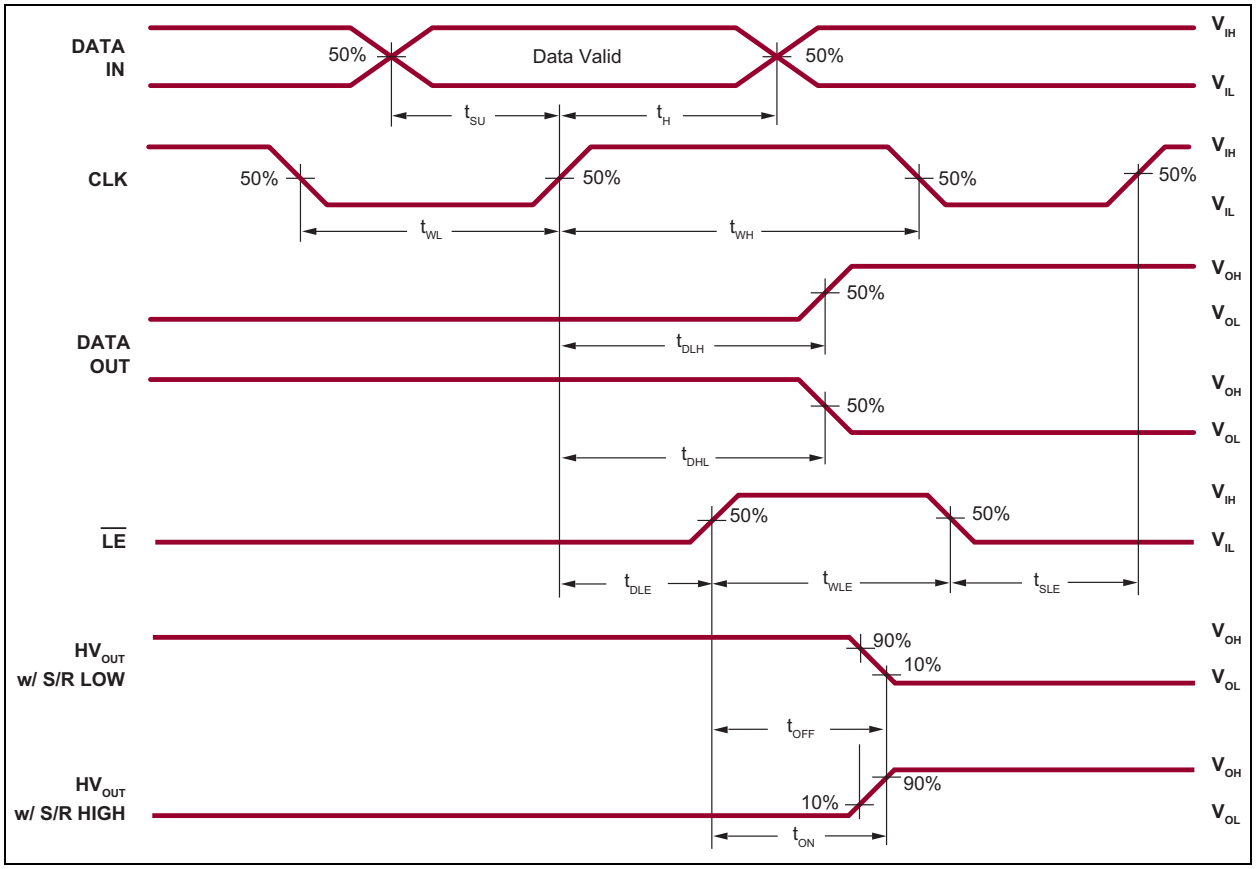
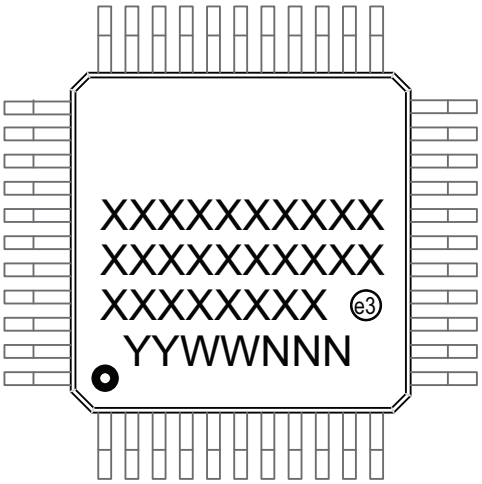


FIGURE 3-2: *Switching Waveforms*

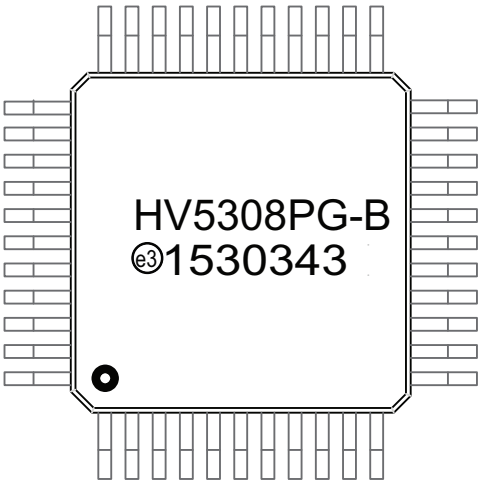
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

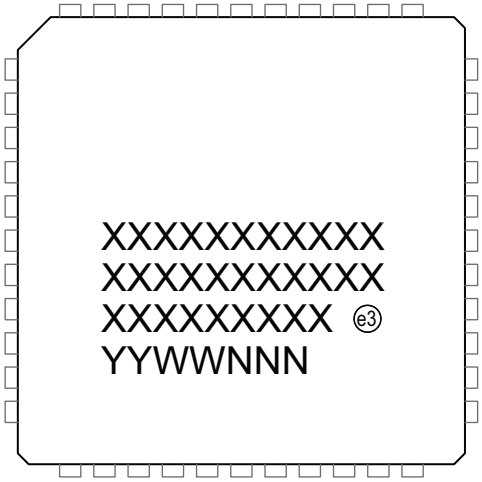
44-lead PQFP



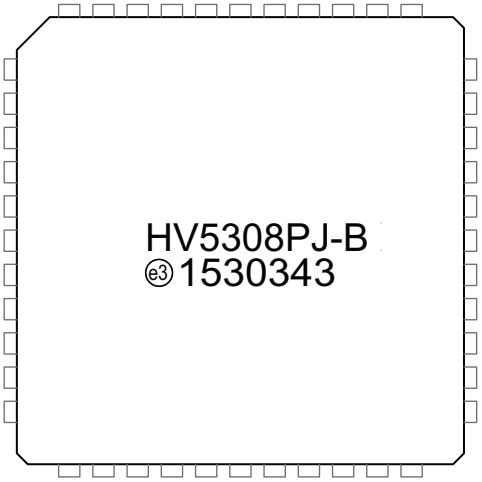
Example



44-lead PLCC



Example

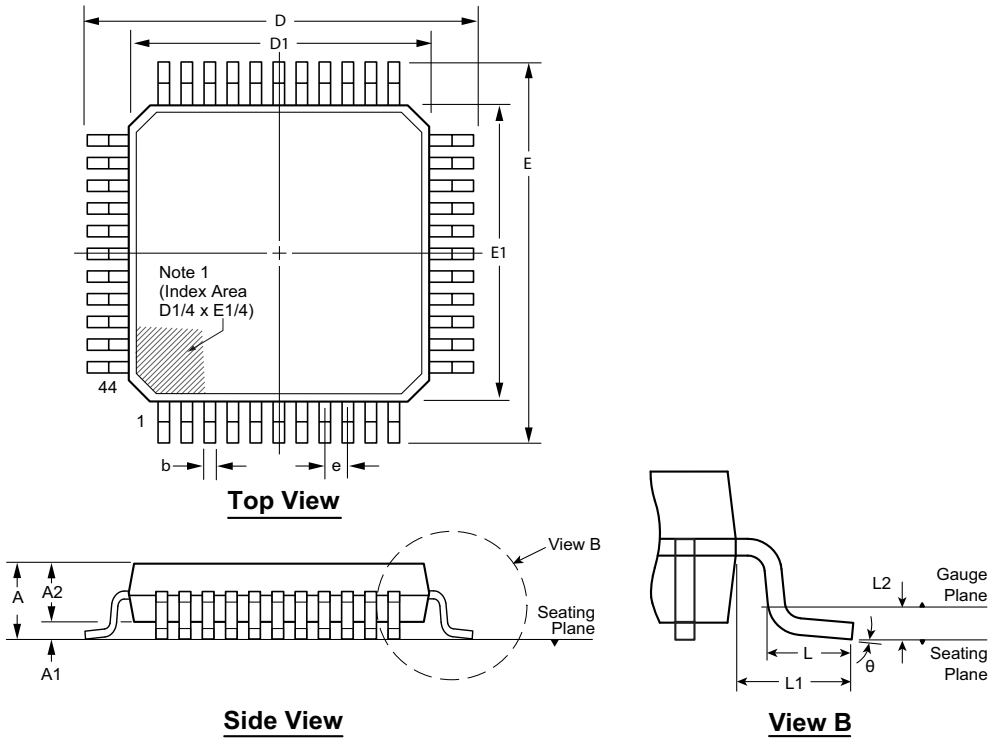


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

44-Lead PQFP Package Outline (PG)

10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

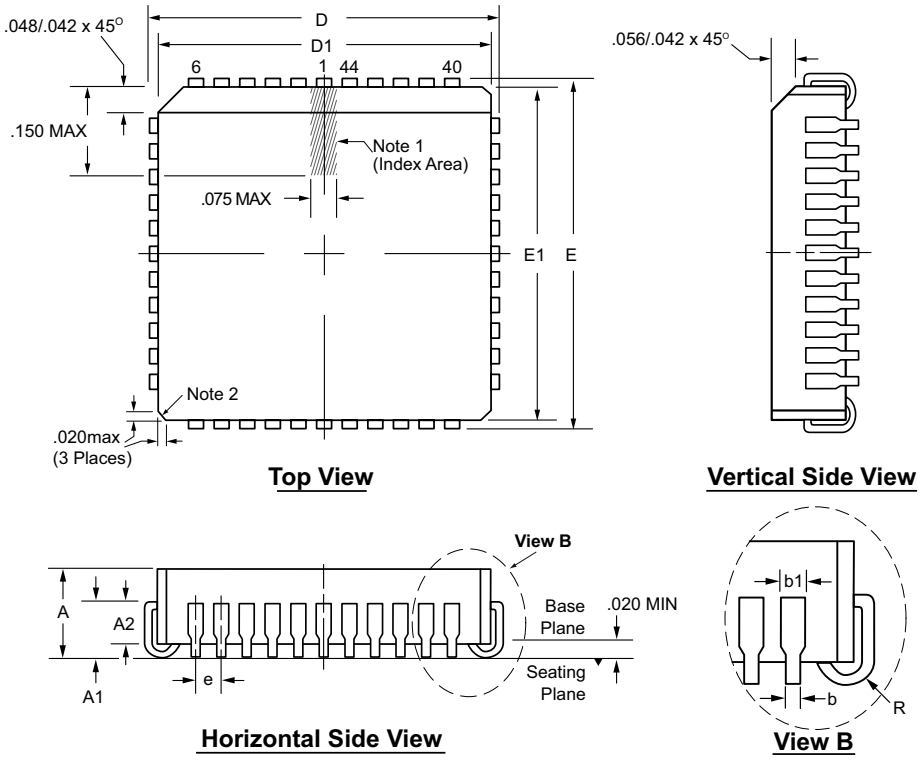
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			3.5°
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7°

JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (December 2015)

- Updated file to Microchip format

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X	-	X
Device	Package Options		Version		Environmental		Media Type

Device:	HV5308 =	32-Channel Serial to Parallel Converter, with High-voltage Push-pull Outputs data shifts in clockwise direction
	HV5408 =	32-Channel Serial to Parallel Converter, with High-voltage Push-pull Outputs data shifts in counter-clockwise direction
Package:	PG =	44-Lead PQFP
	PJ =	44-Lead PLCC
Version	B =	Revision B
Environmental	G =	Lead (Pb)-free/ROHS-compliant package
Media Type:	(blank) =	96/Tray for PG package
	=	27/Tube for PJ package
	M903 =	500/Reel for PG package
	M919 =	500/Reel for PJ package

Examples:

a)	HV5308PG-B-G	Clockwise data shift, 44-Lead PQFP package, 96/Tray
b)	HV5308PG-B-G-M919	Clockwise data shift, 44-Lead PQFP package, 500/Reel
c)	HV5308PJ-B-G	Clockwise data shift, 44-Lead PLCC package, 27/Tube
d)	HV5308PJ-B-G-M903	Clockwise data shift, 44-Lead PLCC package, 500/Reel
e)	HV5408PG-B-G	Counter-clockwise data shift, 44-Lead PQFP package, 96/Tray
f)	HV5408PJ-B-G	Counter-clockwise data shift, 44-Lead PLCC package, 27/Tube

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Korea - Seoul
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