MCP48FEBXX

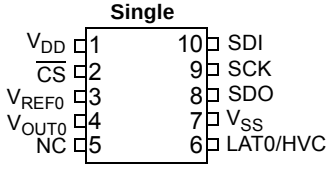
8-/10-/12-Bit Single/Dual Voltage Output Nonvolatile Digital-to-Analog Converters with SPI Interface

Features

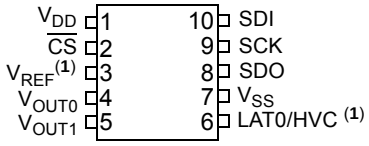
- Operating Voltage Range:
  - 2.7V to 5.5V - full specifications
  - 1.8V to 2.7V - reduced device specifications
- Output Voltage Resolutions:
  - 8-bit: **MCP48FEB0X** (256 Steps)
  - 10-bit: **MCP48FEB1X** (1024 Steps)
  - 12-bit: **MCP48FEB2X** (4096 Steps)
- Rail-to-Rail Output
- Fast Settling Time of 7.8 µs (typical)
- DAC Voltage Reference Source Options:
  - Device V_{DD}
  - External V_{REF} pin (buffered or unbuffered)
  - Internal Band Gap (1.22V typical)
- Output Gain Options:
  - Unity (1x)
  - 2x
- Nonvolatile Memory (EEPROM):
  - User-programmed Power-on Reset (POR)/Brown-out Reset (BOR) output setting, recall and device configuration bits
  - Auto Recall of Saved DAC register setting
  - Auto Recall of Saved Device Configuration (Voltage Reference, Gain, Power-Down)
- Power-on/Brown-out Reset Protection
- Power-Down Modes:
  - Disconnects output buffer (High Impedance)
  - Selection of V_{OUT} pull-down resistors (100 kΩ or 1 kΩ)
- Low Power Consumption:
  - Normal operation: <180 µA (Single), 380 µA (Dual)
  - Power-down operation: 650 nA typical
  - EEPROM write cycle (1.9 mA maximum)
- SPI Interface:
  - Supports '00' and '11' modes
  - Up to 20 MHz writes and 10 MHz reads
  - Input buffers support interfacing to low-voltage digital devices
- Package Types: 10-lead MSOP
- Extended Temperature Range: -40°C to +125°C

Package Types

MCP48FEBx1
MSOP
Single



MCP48FEBx2
MSOP
Dual



Note 1: Associated with both DAC0 and DAC1

General Description

The MCP48FEBXX are Single- and Dual-channel 8-bit, 10-bit, and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with nonvolatile memory and an SPI serial interface.

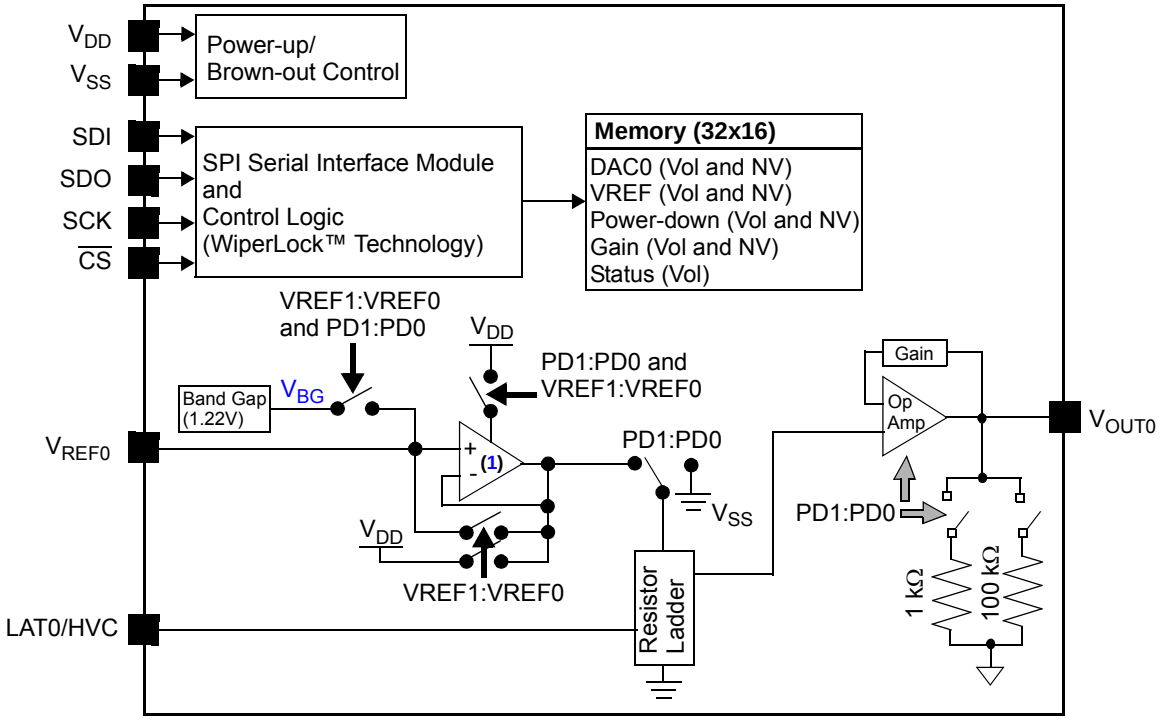
The V_{REF} pin, the device V_{DD} or the internal band gap voltage can be selected as the DAC's reference voltage. When V_{DD} is selected, V_{DD} is connected internally to the DAC reference circuit. When the V_{REF} pin is used, the user can select the output buffer's gain to be 1 or 2. When the gain is 2, the V_{REF} pin voltage should be limited to a maximum of $V_{DD}/2$.

These devices have an SPI-compatible serial interface. Write commands are supported up to 20 MHz while read commands are supported up to 10 MHz.

Applications

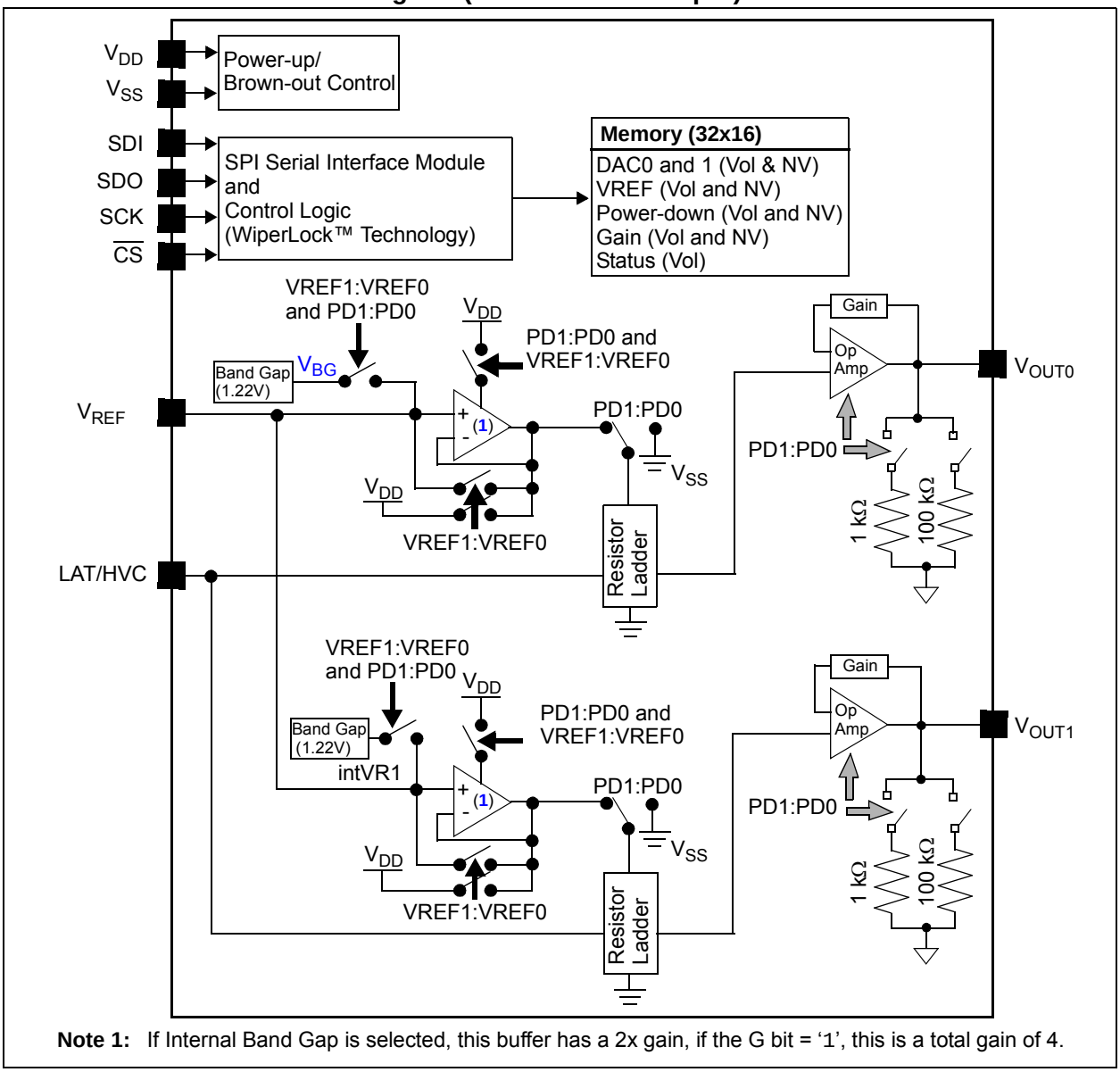
- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems
- Motor Control

MCP48FEBX1 Device Block Diagram (Single-Channel Output)



Note 1: If Internal Band Gap is selected, this buffer has a 2x gain. If the G bit = '1', this is a total gain of 4.

MCP48FEBX2 Device Block Diagram (Dual-Channel Output)



Note 1: If Internal Band Gap is selected, this buffer has a 2x gain, if the G bit = '1', this is a total gain of 4.

Device Features

Device	# of Channels	Resolution (bits)	Control Interface	DAC Output POR/BOR Setting (1)	# of VREF Inputs	Internal band gap ?	# of LAT Inputs	Memory	Specified Operating Range (V_{DD}) (2)
MCP48FEB01	1	8	SPI	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB11	1	10	SPI	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB21	1	12	SPI	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB02	2	8	SPI	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB12	2	10	SPI	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB22	2	12	SPI	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FVB01	1	8	I²C™	7Fh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB11	1	10	I²C	1FFh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB21	1	12	I²C	7FFh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB02	2	8	I²C	7Fh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB12	2	10	I²C	1FFh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB22	2	12	I²C	7FFh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FEB01	1	8	I²C	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB11	1	10	I²C	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB21	1	12	I²C	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB02	2	8	I²C	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB12	2	10	I²C	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB22	2	12	I²C	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V

Note 1: Factory Default value. The DAC output POR/BOR value can be modified via the nonvolatile DAC output register(s) (available only on nonvolatile devices (MCP4XFEBXX)).

2: Analog output performance specified from 2.7V to 5.5V.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Voltage on V_{DD} with respect to V_{SS} ..... -0.6V to +6.5V

Voltage on all pins with respect to V_{SS} ..... -0.6V to V_{DD}+0.3V

Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ on HV pins) ..... ±20 mA

Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA

Maximum current out of V_{SS} pin (Single) ..... 50 mA
(Dual) ..... 100 mA

Maximum current into V_{DD} pin (Single) ..... 50 mA
(Dual) ..... 100 mA

Maximum current sourced by the V_{OUT} pin ..... 20 mA

Maximum current sunk by the V_{OUT} pin ..... 20 mA

Maximum current sunk by the V_{REF} pin ..... 125 µA

Maximum input current source/sunk by SDI, SCK, and $\overline{CS}$ pins ..... 2 mA

Maximum output current sunk by SDO Output pin ..... 25 mA

Total power dissipation (1) ..... 400 mW

Package power dissipation (T_A = +50°C, T_J = +150°C)
MSOP-10 ..... 490 mW

ESD protection on all pins ..... ≥ ±4 kV (HBM)
..... ≥ ±400V (MM)
..... ≥ ±1.5 kV (CDM)

Latch-Up (per JEDEC JESD78A) @ +125°C ..... ±100 mA

Storage temperature ..... -65°C to +150°C

Ambient temperature with power applied ..... -55°C to +125°C

Soldering temperature of leads (10 seconds) ..... +300°C

Maximum Junction Temperature (T_J) ..... +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

DC CHARACTERISTICS

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	V_{DD}	2.7	—	5.5	V	
		1.8	—	2.7	V	DAC operation (reduced analog specifications) and Serial Interface
V_{DD} Voltage (rising) to ensure device Power-on Reset	$V_{POR/BOR}$	—	—	1.7	V	RAM retention voltage (V_{RAM}) < V_{POR} V_{DD} voltages greater than $V_{POR/BOR}$ limit Ensure that device is out of reset.
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	(**Note 3**)			V/ms	
High-Voltage Commands Voltage Range (HVC pin)	V_{HV}	V_{SS}	—	12.5	V	The HVC pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}) (1)
High-Voltage Input Entry Voltage	V_{IHHEN}	9.0	—	—	V	Threshold for Entry into WiperLock Technology
High-Voltage Input Exit Voltage	V_{IHHEX}	—	—	V_{DD} + 0.8V	V	**(Note 2)**
Power-on Reset to Output-Driven Delay	T_{PORD}	—	25	50	µs	V_{DD} rising, V_{DD} > V_{POR}

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 3 POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Supply Current	I_{DD}	—	—	320	µA	Single	1MHz (2)	Serial Interface Active (Not High-Voltage Command) VRxB:VRxA = '01' (6) V_{OUT} is unloaded, V_{DD} = 5.5V Volatile DAC Register = 000h
		—	—	910	µA		10MHz (2)	
		—	—	1.7	mA		20MHz	
		—	—	510	µA	Dual	1MHz (2)	
		—	—	1.1	mA		10MHz (2)	
		—	—	1.85	mA		20MHz	
		—	—	250	µA	Single	1MHz (2)	Serial Interface Active (Not High-Voltage Command) VRxB:VRxA = '10' (4) V_{OUT} is unloaded. V_{REF} = V_{DD} = 5.5V Volatile DAC Register = 000h
		—	—	840	µA		10MHz (2)	
		—	—	1.65	mA		20MHz (2)	
		—	—	380	µA	Dual	1MHz (2)	
		—	—	970	µA		10MHz (2)	
		—	—	1.75	mA		20MHz (2)	
		—	—	180	µA	Single	Serial Interface Inactive (2) (Not High-Voltage Command) VRxB:VRxA = '00' SCK = SDI = V_{SS} V_{OUT} is unloaded. Volatile DAC Register = 000h	
		—	—	380	µA	Dual		
		—	—	180	µA	Single	Serial Interface Inactive (2) (Not High-Voltage Command) VRxB:VRxA = '11', V_{REF} = V_{DD} SCK = SDI = V_{SS} V_{OUT} is unloaded. Volatile DAC Register = 000h	
		—	—	380	µA	Dual		
		—	—	1.9	mA	EE Write Current V_{REF} = V_{DD} = 5.5V (After write, Serial Interface is Inactive.) Write all 0's to non-volatile DAC 0 (address 10h). V_{OUT} pins are unloaded.		
		—	145	180	µA	Single	HVC = 12.5V (High-Voltage Command) Serial Interface Inactive V_{REF} = V_{DD} = 5.5V, LAT/HVC = V_{IHH} DAC registers = 000h V_{OUT} pins are unloaded.	
		—	260	400	µA	Dual		
Power-Down Current	I_{DDP}	—	0.65	3.8	µA	PDxB:PDxA = '01' (5), V_{OUT} not connected		

Note 2 This parameter is ensured by characterization.

Note 4 Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = '10'.

Note 5 The PDxB:PDxA = '01', '10', and '11' configurations should have the same current.

Note 6 By design, this is the worst-case current mode.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Resistor Ladder Resistance	R_L	100	140	180	kΩ	1.8V ≤ V_{DD} ≤ 5.5V V_{REF} ≥ 1.0V (7)
Resolution (# of Resistors and # of Taps) (see **B.1 "Resolution"**)	N	256			Taps	8-bit — No Missing Codes
		1024			Taps	10-bit — No Missing Codes
		4096			Taps	12-bit — No Missing Codes
Nominal V_{OUT} Match (11)	$\lvert V_{OUT} - V_{OUTMEAN} \rvert / V_{OUTMEAN}$	—	0.5	1.0	%	2.7V ≤ V_{DD} ≤ 5.5V (2)
		—	—	1.2	%	1.8V (2)
V_{OUT} Tempco (see **B.19 "V_{OUT} Temperature Coefficient"**)	$\Delta V_{OUT}/\Delta T$	—	15	—	ppm/°C	Code = Mid-scale (7Fh, 1FFh or 7FFh)
V_{REF} pin Input Voltage Range	V_{REF}	V_{SS}	—	V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V (1)

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 7 Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = '10') to V_{SS} pin. For dual-channel devices (MCP48FEBX2), this is the effective resistance of the each resistor ladder. The resistance measurement is of the two resistor ladders measured in parallel.

Note 11 Variation of one output voltage to mean output voltage.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Zero-Scale Error (see **B.5 "Zero-Scale Error (EZS)"**) (Code = 000h)	E_{ZS}	—	—	0.75	LSb	8-bit	VRxB:VRxA = '11', Gx = '0' V_{REF} = V_{DD}, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', Gx = '0' V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01', Gx = '0', No Load
		—	—	3	LSb	10-bit	VRxB:VRxA = '11', Gx = '0' V_{REF} = V_{DD}, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', Gx = '0' V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01', Gx = '0' No Load
		—	—	12	LSb	12-bit	VRxB:VRxA = '11', Gx = '0' V_{REF} = V_{DD}, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', Gx = '0' V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01', Gx = '0' No Load
Offset Error (see **B.7 "Offset Error (EOS)"**)	E_{OS}	-15	±1.5	+15	mV	VRxB:VRxA = '00' Gx = '0' No Load	
Offset Voltage Temperature Coefficient	V_{OSTC}	—	±10	—	µV/°C		

Note 2 This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Full-Scale Error (see **B.4 "Full-Scale Error (EFS)"**)	E_{FS}	—	—	4.5	LSb	8-bit	Code = FFh, VRxB:VRxA = '11' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFh, VRxB:VRxA = '10' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFh, VRxB:VRxA = '01' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFh, VRxB:VRxA = '00' No Load
		—	—	18	LSb	10-bit	Code = 3FFh, VRxB:VRxA = '11' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = 3FFh, VRxB:VRxA = '10' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = 3FFh, VRxB:VRxA = '01' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = 3FFh, VRxB:VRxA = '00' No Load
		—	—	70	LSb	12-bit	Code = FFFh, VRxB:VRxA = '11' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFFh, VRxB:VRxA = '10' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFFh, VRxB:VRxA = '01' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFFh, VRxB:VRxA = '00' No Load

Note 2 This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Gain Error (see **B.9 "Gain Error (EG)"**)[8]	E_G	-1.0	±0.1	+1.0	% of FSR	8-bit	Code = 250, No Load VRxB:VRxA = '00' Gx = '0'
		-1.0	±0.1	+1.0	% of FSR	10-bit	Code = 1000, No Load VRxB:VRxA = '00' Gx = '0'
		-1.0	±0.1	+1.0	% of FSR	12-bit	Code = 4000, No Load VRxB:VRxA = '00' Gx = '0'
Gain-Error Drift (see **B.10 "Gain-Error Drift (EGD)"**)	ΔG/°C	—	-3	—	ppm/°C		

Note 2 This parameter is ensured by characterization.

Note 8 This gain error does not include offset error.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Integral Nonlinearity (see **B.11 "Integral Nonlinearity (INL)"**) (10)	INL	-0.5	±0.1	+0.5	LSb	8-bit	VRxB:VRxA = '10' (codes: 6 to 250) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V V_{REF} = 1.0V
		-1.5	±0.4	+1.5	LSb	10-bit	VRxB:VRxA = '10' (codes: 25 to 1000) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V V_{REF} = 1.0V
		-6	±1.5	+6	LSb	12-bit	VRxB:VRxA = '10' (codes: 100 to 4000) V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		V_{DD} = 1.8V V_{REF} = 1.0V

Note 2 This parameter is ensured by characterization.

Note 10 Code range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, codes 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**		**Conditions**
Differential Nonlinearity (see **B.12 "Differential Nonlinearity (DNL)"**)(10)	DNL	-0.25	±0.0125	+0.25	LSb	8-bit	VRxB:VRxA = '10' (codes: 6 to 250) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		V_{DD} = 1.8V
		-0.5	±0.05	+0.5	LSb	10-bit	VRxB:VRxA = '10' (codes: 25 to 1000) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		V_{DD} = 1.8V
		-1.0	±0.2	+1.0	LSb	12-bit	VRxB:VRxA = '10' (codes: 100 to 4000) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		V_{DD} = 1.8V

Note 2 This parameter is ensured by characterization.

Note 10 Code range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, codes 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
-3 dB Bandwidth (see **B.16 "-3 dB Bandwidth"**)	BW	—	200	—	kHz	V_{REF} = 2.048V ± 0.1V VRxB:VRxA = '10', Gx = '0'
		—	100	—	kHz	V_{REF} = 2.048V ± 0.1V VRxB:VRxA = '10', Gx = '1'
Output Amplifier						
Minimum Output Voltage	$V_{OUT(MIN)}$	—	0.01	—	V	1.8V ≤ V_{DD} < 5.5V Output Amplifier's minimum drive
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{DD} – 0.04	—	V	1.8V ≤ V_{DD} < 5.5V Output Amplifier's maximum drive
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF R_L = ∞
Slew Rate (9)	SR	—	0.44	—	V/µs	R_L = 5 kΩ
Short-Circuit Current	I_{SC}	3	9	14	mA	DAC code = Full Scale
Internal Band Gap						
Band Gap Voltage	V_{BG}	1.18	1.22	1.26	V	
Band Gap Voltage Temperature Coefficient	V_{BGTC}	—	15	—	ppm/°C	
Operating Range (V_{DD})		2.0	—	5.5	V	V_{REF} pin voltage stable
		2.2	—	5.5	V	V_{OUT} output linear
External Reference (V_{REF})						
Input Range (1)	V_{REF}	V_{SS}	—	V_{DD} – 0.04	V	VRxB:VRxA = '11' (Buffered mode)
		V_{SS}	—	V_{DD}	V	VRxB:VRxA = '10' (Unbuffered mode)
Input Capacitance	C_{REF}	—	1	—	pF	VRxB:VRxA = '10' (Unbuffered mode)
Total Harmonic Distortion (1)	THD	—	-64	—	dB	V_{REF} = 2.048V ± 0.1V VRxB:VRxA = '10', Gx = '0' Frequency = 1 kHz
Dynamic Performance						
Major Code Transition Glitch (see **B.14 "Major-Code Transition Glitch"**)		—	45	—	nV-s	1 LSb change around major carry (7FFh to 800h)
Digital Feedthrough (see **B.15 "Digital Feed-through"**)		—	<10	—	nV-s	

Note 1 This parameter is ensured by design.

Note 9 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Digital Inputs/Outputs ($\overline{CS}$, SCK, SDI, SDO, $\overline{LAT0}$/HVC)						
Schmitt Trigger High-Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	2.7V ≤ V_{DD} ≤ 5.5V
		0.5 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 2.7V
Schmitt Trigger Low-Input Threshold	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_{DD}	—	V	
Output Low Voltage	V_{OL}	V_{SS}	—	0.3 V_{DD}	V	I_{OL} = 5 mA, V_{DD} = 5.5V
		V_{SS}	—	0.3 V_{DD}	V	I_{OL} = 1 mA, V_{DD} = 1.8V
Output High Voltage	V_{OH}	0.7V_{DD}	—	V_{DD}	V	I_{OH} = -2.5 mA, V_{DD} = 5.5V
		0.7V_{DD}	—	V_{DD}	V	I_{OH} = -1 mA, V_{DD} = 1.8V
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 20 MHz

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
RAM Value							
Value Range	N	0h	—	FFh	hex	8-bit	
		0h	—	3FFh	hex	10-bit	
		0h	—	FFFh	hex	12-bit	
DAC Register POR/BOR Value	N	See **Table 4-2**			hex	8-bit	
		See **Table 4-2**			hex	10-bit	
		See **Table 4-2**			hex	12-bit	
PDCON Initial Factory Setting		See **Table 4-2**			hex		
EEPROM							
Endurance	EN_{EE}	—	1M	—	Cycles	**Note 1**, **Note 2**	
Data Retention	DR_{EE}	—	200	—	Years	At +25°C (**1**), (**2**)	
EEPROM Range	N	0h	—	FFh	hex	8-bit	DACx Register(s)
		0h	—	3FFh	hex	10-bit	DACx Register(s)
		0h	—	FFFh	hex	12-bit	DACx Register(s)
Initial Factory Setting	N	See **Table 4-2**					
EEPROM Programming Write Cycle Time	t_{WC}	—	11	16	ms	V_{DD} = +1.8V to 5.5V	
Power Requirements							
Power Supply Sensitivity (**B.17 "Power-Supply Sensitivity (PSS)"**)	PSS	—	0.002	0.005	%/%	8-bit	Code = 7Fh
		—	0.002	0.005	%/%	10-bit	Code = 1FFh
		—	0.002	0.005	%/%	12-bit	Code = 7FFh

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = '10'.
5. The PDxB:PDxA = '01', '10', and '11' configurations should have the same current.
6. By design, this is the worst-case current mode.
7. Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = '10') to V_{SS} pin. For dual-channel devices (MCP48FEBX2), this is the effective resistance of the each resistor ladder. The resistance measurement is of the two resistor ladders measured in parallel.
8. This gain error does not include offset error.
9. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
10. Code range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, codes 100 to 4000.
11. Variation of one output voltage to mean output voltage.

1.1 Reset, Power-Down, and SPI Mode Timing Waveforms and Requirements

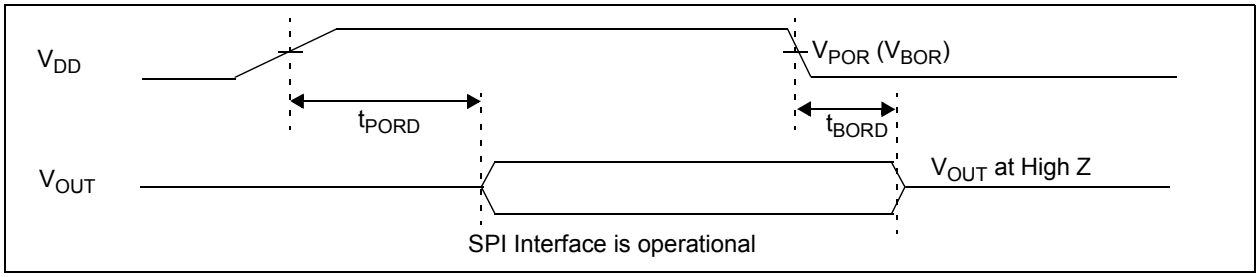


FIGURE 1-1: *Power-on and Brown-out Reset Waveforms.*

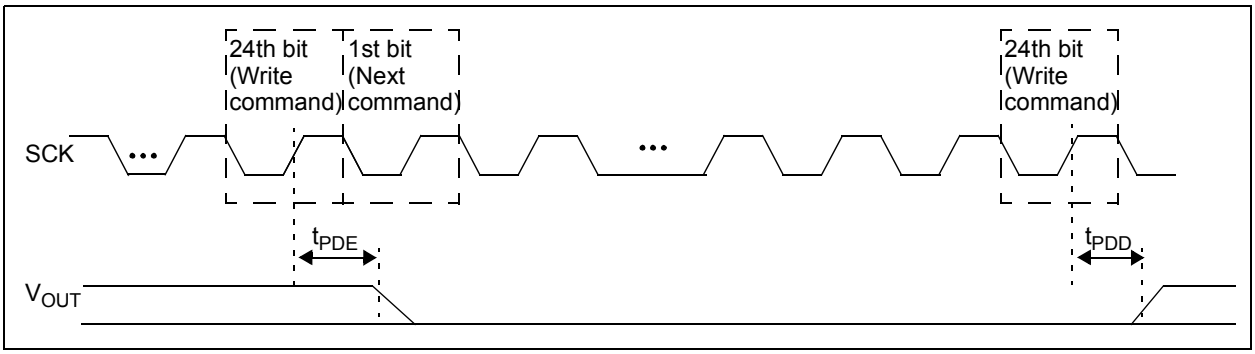


FIGURE 1-2: *SPI Power-Down Command Waveforms.*

TABLE 1-1: RESET AND POWER-DOWN TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +1.8V to 5.5V, V_{SS} = 0V R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power-on Reset Delay	t_{PORD}	—	60	—	µs	
Brown-out Reset Delay	t_{BORD}	—	45	—	µs	V_{DD} transitions from $V_{DD(MIN)} \rightarrow > V_{POR}$ V_{OUT} driven to V_{OUT} disabled
Power-Down Output Disable Time Delay	T_{PDD}	—	10.5	—	µs	PDxB:PDxA = '11', '10', or '01' → "00" started from falling edge of the SCK at the end of the 24th clock cycle. Volatile DAC Register = FFh, V_{OUT} = 10 mV. V_{OUT} not connected.
Power-Down Output Enable Time Delay	T_{PDE}	—	1	—	µs	PDxB:PDxA = "00" → '11', '10', or '01' started from falling edge of the SCK at the end of the 24th clock cycle. V_{OUT} = V_{OUT} - 10 mV. V_{OUT} not connected.

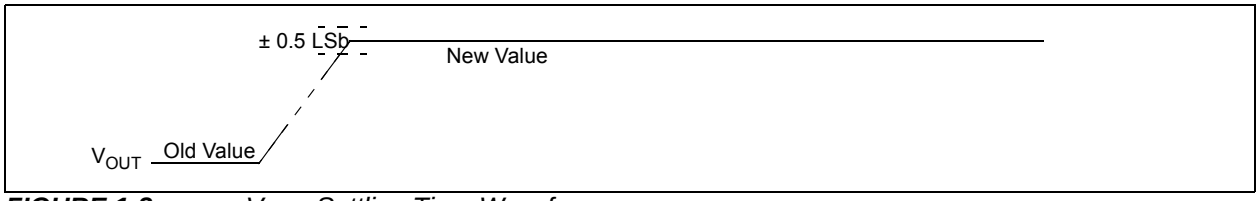


FIGURE 1-3: *V_{OUT} Settling Time Waveform.*

TABLE 1-2: V_{OUT} SETTLING TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +1.8V to 5.5V, V_{SS} = 0V R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_{OUT} Settling Time (±0.5LSb error band, C_L = 100 pF) (see **B.13 "Settling Time"**)	t_S	—	7.8	—	µs	8-bit	Code = 40h → C0h; C0h → 40h (3)
		—	7.8	—	µs	10-bit	Code = 100h → 300h; 300h → 100h (3)
		—	7.8	—	µs	12-bit	Code = 400h → C00h; C00h → 400h (3)

Note 3 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).

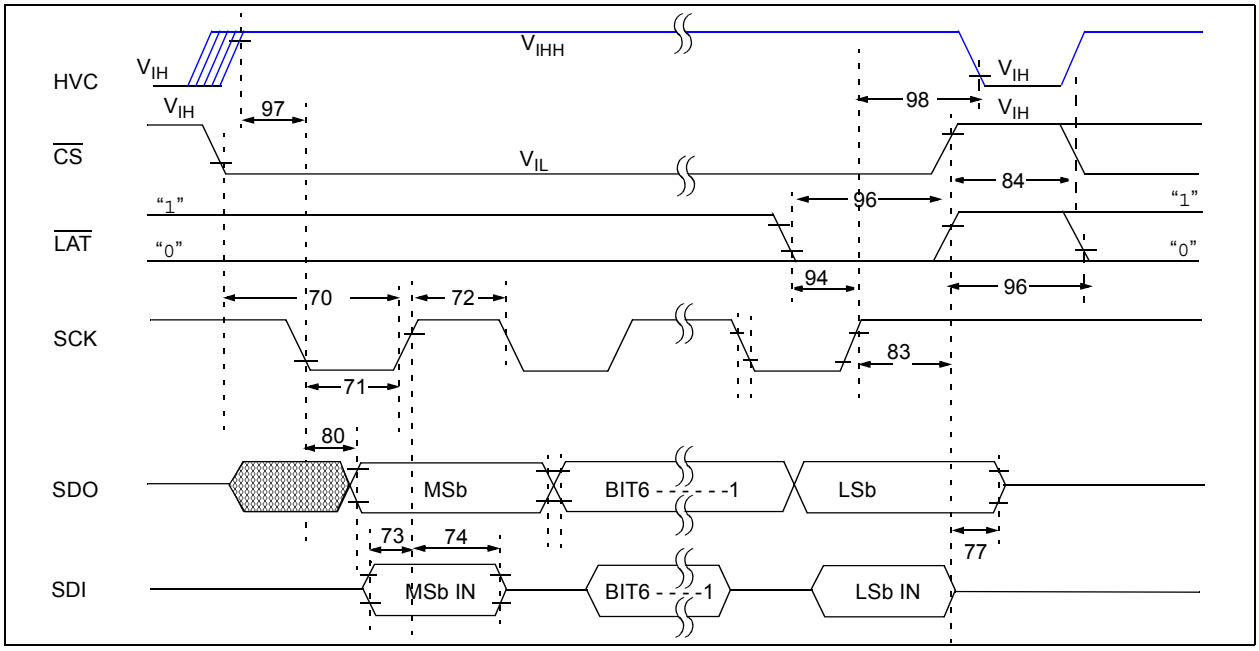


FIGURE 1-4: *SPI Timing (Mode = 11) Waveforms.*

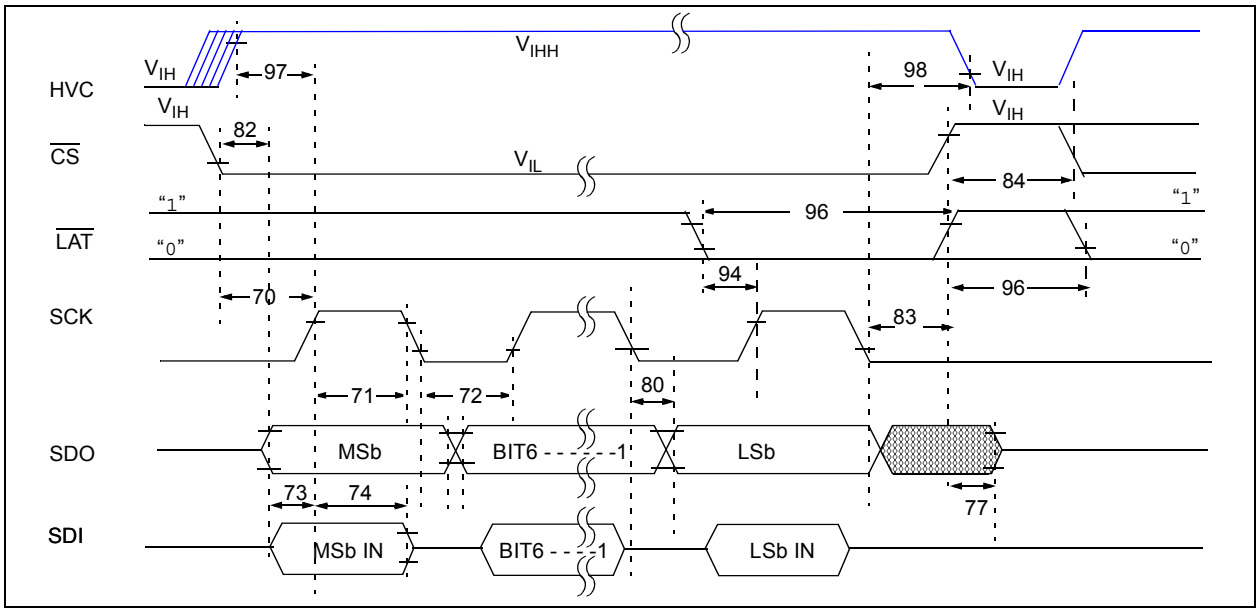


FIGURE 1-5: *SPI Timing (Mode = 00) Waveforms.*

TABLE 1-3: SPI REQUIREMENTS (MODE = 11)

SPI AC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Operating Voltage range is described in **DC Characteristics**.				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	F_{SCK}	SCK input frequency	—	10	MHz	V_{DD} = 2.7V to 5.5V (Read Command)
			—	20	MHz	V_{DD} = 2.7V to 5.5V (All Other Commands)
			—	1	MHz	V_{DD} = 1.8V to 2.7V
70	TcsA2scH	$\overline{CS}$ Active (V_{IL}) to command's 1st SCK↑ input	60	—	ns	
71	TscH	SCK input high time	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
72	TscL	SCK input low time	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
73	TdiV2scH	Setup time of SDI input to SCK↑ edge	10	—	ns	
74	TscH2diL	Hold time of SDI input from SCK↑ edge	20	—	ns	
77	TcsH2DOZ	$\overline{CS}$ Inactive (V_{IH}) to SDO output hi-impedance	—	50	ns	**Note 1**
80	TscL2doV	SDO data output valid after SCK↓ edge	—	45	ns	V_{DD} = 2.7V to 5.5V
			—	170	ns	V_{DD} = 1.8V to 2.7V
83	TscH2csL	$\overline{CS}$ Inactive (V_{IH}) after SCK↑ edge	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		µs	V_{DD} = 1.8V to 2.7V
84	TcsH	$\overline{CS}$ high time (V_{IH})	50	—	ns	
94	T_{LATSU}	$\overline{LAT}$ ↓ to SCK↑ (write data 24th bit) setup time	20	—	ns	Write Data transferred (4)
96	T_{LAT}	$\overline{LAT}$ high or low time	20	—	ns	
97	T_{HVCSU}	HVC ↑ to SCK ↓ (1st data bit) (HVC setup time)	0	—	ns	High-Voltage Commands(1)
98	T_{HVCHD}	SCK ↑ (last bit of command (8th or 24th bit)) to HVC ↓ (HVC hold time)	25	—	ns	High-Voltage Commands(1)

Note 1 This parameter is ensured by design.

Note 4 The transition of the LAT signal must occur 10 ns before the rising edge of the 24th SCK signal (Spec 94) or the current register data value may not be transferred to the output latch (VOUT) before the register is overwritten with the new value.

TABLE 1-4: SPI REQUIREMENTS (MODE = 00)

SPI AC Characteristics			Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Operating Voltage range is described in **DC Characteristics**.			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	F_{SCK}	SCK input frequency	—	10	MHz	V_{DD} = 2.7V to 5.5V (Read Command)
			—	20	MHz	V_{DD} = 2.7V to 5.5V (All Other Commands)
			—	1	MHz	V_{DD} = 1.8V to 2.7V
70	TcsA2scH	$\overline{CS}$ Active (V_{IL}) to SCK↑ input	60	—	ns	
71	TscH	SCK input high time	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
72	TscL	SCK input low time	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
73	TDIV2scH	Setup time of SDI input to SCK↑ edge	10	—	ns	
74	TscH2DIL	Hold time of SDI input from SCK↑ edge	20	—	ns	
77	TcsH2DOZ	$\overline{CS}$ Inactive (V_{IH}) to SDO output hi-impedance	—	50	ns	**Note 1**
80	TscL2DOV	SDO data output valid after SCK↓ edge	—	45	ns	V_{DD} = 2.7V to 5.5V
			—	170	ns	V_{DD} = 1.8V to 2.7V
82	TssL2doV	SDO data output valid after $\overline{CS}$ Active (V_{IL})	—	70	ns	
83	TscH2csL	$\overline{CS}$ Inactive (V_{IH}) after SCK↓ edge	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		µs	V_{DD} = 1.8V to 2.7V
84	TcsH	$\overline{CS}$ high time (V_{IH})	50	—	ns	
94	T_{LATSU}	$\overline{LAT}$ ↓ to SCK↑ (write data 24th bit) setup time	10	—	ns	Write Data transferred (4)
96	T_{LAT}	$\overline{LAT}$ high or low time	50	—	ns	
97	T_{HVCSU}	HVC ↑ to SCK ↑ (1st data bit) (HVC setup time)	0	—	ns	High-Voltage Commands (1)
98	T_{HVCHD}	SCK ↓ (last bit of command (8th or 24th bit)) to HVC ↓ (HVC hold time)	25	—	ns	High-Voltage Commands (1)

Note 1 This parameter is ensured by design.

Note 4 The transition of the LAT signal must occur 10 ns before the rising edge of the 24th SCK signal (Spec 94) or the current register data value may not be transferred to the output latch (VOUT) before the register is overwritten with the new value.

Timing Table Notes:

1. This parameter is ensured by design.
2. This parameter ensured by characterization.
3. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
4. The transition of the LAT signal must occur 10 ns before the rising edge of the 24th SCK signal (Spec 94) or the current register data value may not be transferred to the output latch (V_{OUT}) before the register is overwritten with the new value.

Temperature Specifications

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 10LD-MSOP	θ_{JA}	—	202	—	°C/W	

Note 1: The MCP48FEBXX devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of +150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note: The device Performance Curves are available in a separate document. This is done to keep the file size of this PDF document less than the 10 MB file attachment limit of many mail servers.
The MCP48FXBXX Performance Curves document is literature number **DS20005440**, and can be found on the Microchip website. Look on the MCP48FEBXX product page under “Documentation and Software”, in the Data Sheets category.

NOTES:

3.0 PIN DESCRIPTIONS

Overviews of the pin functions are provided in **Sections 3.1 "Positive Power Supply Input (V_{DD})"** through **Section 3.10 "SPI - Serial Clock Pin (SCK)"**. The descriptions of the pins for the single-DAC output device are listed in Table 3-1, and descriptions for the dual-DAC output device are listed in Table 3-2.

TABLE 3-1: MCP48FEBX1 (Single-DAC) Pinout Description

Pin				Standard Function
MSOP-10LD	Symbol	I/O	Buffer Type	
1	V_{DD}	—	P	Supply Voltage Pin
2	$\overline{CS}$	I	ST	SPI Chip Select Pin
3	V_{REF0}	A	Analog	Voltage Reference Input Pin
4	V_{OUT0}	A	Analog	Buffered Analog Voltage Output Pin
5	NC	—	—	Not Internally Connected
6	LAT0/HVC	I	HV ST	DAC Register Latch/High-Voltage Command Pin. Latch Pin allows the value in the Serial Shift Register to transfer to the volatile DAC register. High-Voltage command allows User Configuration Bits to be written.
7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
8	SDO	O	—	SPI Serial Data Output Pin
9	SCK	I	ST	SPI Serial Clock Pin
10	SDI	I	ST	SPI Serial Data Input Pin

Legend: A = Analog, I = Input, ST = Schmitt Trigger, O = Output, HV = High Voltage, I/O = Input/Output, P = Power

TABLE 3-2: MCP48FEBX2 (Dual-DAC) Pinout Description

Pin				Standard Function
MSOP-10LD	Symbol	I/O	Buffer Type	
1	V_{DD}	—	P	Supply Voltage Pin
2	$\overline{CS}$	I	ST	SPI Chip Select Pin
3	V_{REF}	A	Analog	Voltage Reference Input Pin (for DAC0 and DAC1)
4	V_{OUT0}	A	Analog	Buffered Analog Voltage Output 0 Pin
5	V_{OUT1}	A	Analog	Buffered Analog Voltage Output 1 Pin
6	LAT0/HVC	I	HV ST	DAC Register Latch/High-Voltage Command Pin. Latch Pin allows the value in the Serial Shift Register to transfer to the volatile DAC register (for DAC0 and DAC1). High-Voltage command allows User Configuration Bits to be written.
7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
8	SDO	O	—	SPI Serial Data Output Pin
9	SCK	I	ST	SPI Serial Clock Pin
10	SDI	I	ST	SPI Serial Data Input Pin

Legend: A = Analog, I = Input, ST = Schmitt Trigger, O = Output, HV = High Voltage, I/O = Input/Output, P = Power

3.1 Positive Power Supply Input (V_{DD})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS}.

The power supply at the V_{DD} pin should be as clean as possible for a good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate noise present in application boards.

3.2 Voltage Reference Pin (V_{REF})

The V_{REF} pin is either an input or an output. When the DAC's voltage reference is configured as the V_{REF} pin, the pin is an input. When the DAC's voltage reference is configured as the internal band gap, the pin is an output.

When the DAC's voltage reference is configured as the V_{REF} pin, there are two options for this voltage input:

- V_{REF} pin voltage buffered
- V_{REF} pin voltage unbuffered

The buffered option is offered in cases where the external reference voltage does not have sufficient current capability to not drop its voltage when connected to the internal resistor ladder circuit.

When the DAC's voltage reference is configured as the device V_{DD}, the V_{REF} pin is disconnected from the internal circuit.

When the DAC's voltage reference is configured as the internal band gap, the V_{REF} pin's drive capability is minimal, so the output signal should be buffered.

See **Section 5.2 "Voltage Reference Selection"** and Register 4-2 for more details on the configuration bits.

3.3 Analog Output Voltage Pin (V_{OUT})

V_{OUT} is the DAC analog voltage output pin. The DAC output has an output amplifier. The DAC output range is dependent on the selection of the voltage reference source (and potential Output Gain selection). These are:

- Device V_{DD} - The full-scale range of the DAC output is from V_{SS} to approximately V_{DD}.
- V_{REF} pin - The full-scale range of the DAC output is from V_{SS} to $G * V_{RL}$, where G is the gain selection option (1x or 2x).
- Internal Band Gap - The full-scale range of the DAC output is from V_{SS} to $G * (2 * V_{BG})$, where G is the gain selection option (1x or 2x).

In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 100 kΩ, or open. The Power-Down Selection bits settings are shown in Register 4-3 and Table 5-5.

3.4 No Connect (NC)

The NC pin is not connected to the device.

3.5 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.6 Latch Pin (LAT)/High-Voltage Command (HVC)

The LAT pin is used to force the transfer of the DAC register's shift register to the DAC output register. This allows DAC outputs to be updated at the same time.

The update of the VRxB:VRxA, PDxB:PDxA and Gx bits are also controlled by the LAT pin state.

The HVC pin allows the device's nonvolatile user configuration bits to be programmed when the HVC pin is greater than the V_{IHH} entry voltage.

3.7 SPI - Chip Select Pin ($\overline{CS}$)

The $\overline{CS}$ pin enables/disables the serial interface. The serial interface must be enabled for the SPI commands to be received by the device.

Refer to **Section 6.2 "SPI Serial Interface"** for more details of SPI Serial Interface communication.

The NC pin is not connected to the device.

3.8 SPI - Serial Data In Pin (SDI)

The SDI pin is the serial data input pin of the SPI interface. The SDI pin is used to read the DAC registers and configuration bits.

Refer to **Section 6.2 "SPI Serial Interface"** for more details of SPI Serial Interface communication.

3.9 SPI - Serial Data Out Pin (SDO)

The SDO pin is the serial data output pin of the SPI interface. The SDO pin is used to write the DAC registers and configuration bits.

Refer to **Section 6.2 "SPI Serial Interface"** for more details of SPI Serial Interface communication.

3.10 SPI - Serial Clock Pin (SCK)

The SCK pin is the serial clock pin of the SPI interface. The MCP48FEBXX SPI Interface only accepts external serial clocks.

Refer to **Section 6.2, SPI Serial Interface** for more details of SPI Serial Interface communication.

4.0 GENERAL DESCRIPTION

The MCP48FEBX1 (MCP48FEB01, MCP48FEB11, and MCP48FEB21) devices are single-channel voltage output devices. The MCP48FEBX2 (MCP48FEB02, MCP48FEB12, and MCP48FEB22) devices are dual-channel voltage output devices.

These devices are offered with 8-bit (MCP48FEB0X), 10-bit (MCP48FEB1X) and 12-bit (MCP48FEB2X) resolution and include nonvolatile memory (EEPROM), an SPI serial interface and a write latch (LAT) pin to control the update of the written DAC value to the DAC output pin.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software-selectable voltage reference source. The source can be either the device's internal V_{DD}, an external V_{REF} pin voltage (buffered or unbuffered) or an internal band gap voltage source.

The DAC output is buffered with a low power and precision output amplifier (op amp). This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain (1x or 2x) of the output buffer is software configurable.

This device also has user-programmable nonvolatile memory (EEPROM), which allows the user to save the desired POR/BOR value of the DAC register and device configuration bits. High-voltage lock bits can be used to ensure that the devices output settings are not accidentally modified.

The devices operate from a single supply voltage. This voltage is specified from 2.7V to 5.5V for full specified operation, and from 1.8V to 5.5V for digital operation. The devices operate between 1.8V and 2.7V, but some device parameters are not specified.

The main functional blocks are:

- **Power-on Reset/Brown-out Reset (POR/BOR)**
- **Device Memory**
- **Resistor Ladder**
- **Output Buffer/V_{OUT} Operation**
- **Internal Band Gap (Voltage Reference)**
- **SPI Serial Interface Module**

4.1 Power-on Reset/Brown-out Reset (POR/BOR)

The internal Power-on Reset (POR)/Brown-out Reset (BOR) circuit monitors the power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events. The device's RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

POR occurs as the voltage is rising (typically from 0V), while BOR occurs as the voltage is falling (typically from $V_{DD(MIN)}$ or higher).

The POR and BOR trip points are at the same voltage, and the condition is determined by whether the V_{DD} voltage is rising or falling (see Figure 4-1). What occurs is different depending on whether the reset is a POR or BOR.

When V_{POR}/V_{BOR} < V_{DD} < 2.7V, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its EEPROM and reading and writing to its volatile memory if the proper serial command is executed.

4.1.1 POWER-ON RESET

The Power-on Reset is the case where the device V_{DD} is having power applied to it from the V_{SS} voltage level. As the device powers up, the V_{OUT} pin will float to an unknown value. When the device's V_{DD} is above the transistor threshold voltage of the device, the output will start being pulled low. After the V_{DD} is above the POR/BOR trip point (V_{BOR}/V_{POR}), the resistor network's wiper will be loaded with the POR value (mid-scale). The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered-up, the user can update the device memory.

When the rising V_{DD} voltage crosses the V_{POR} trip point, the following occurs:

- Nonvolatile DAC register value is latched into volatile DAC register
- Nonvolatile configuration bit values are latched into volatile configuration bits
- POR Status bit is set ('1')
- The Reset Delay Timer (t_{PORD}) starts; when the reset delay timer (t_{PORD}) times out, the SPI serial interface is operational. During this delay time, the SPI interface will not accept commands.
- The Device Memory Address pointer is forced to 00h.

The analog output (V_{OUT}) state will be determined by the state of the volatile configuration bits and the DAC register. This is called a Power-on Reset (event).

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

4.1.2 BROWN-OUT RESET

The Brown-out Reset occurs when a device had power applied to it and that power (voltage) drops below the specified range.

When the falling V_{DD} voltage crosses the V_{POR} trip point (BOR event), the following occurs:

- Serial Interface is disabled
- EEPROM Writes are disabled
- Device is forced into a Power-Down state (PDxB:PDxA = '11'). Analog circuitry is turned off.
- Volatile DAC Register is forced to 000h
- Volatile configuration bits VRxB:VRxA and Gx are forced to '0'

If the V_{DD} voltage decreases below the V_{RAM} voltage, all volatile memory may become corrupted.

As the voltage recovers above the V_{POR}/V_{BOR} voltage, see **Section 4.1.1 "Power-on Reset"**.

Serial commands not completed due to a brown-out condition may cause the memory location (volatile and nonvolatile) to become corrupted.

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

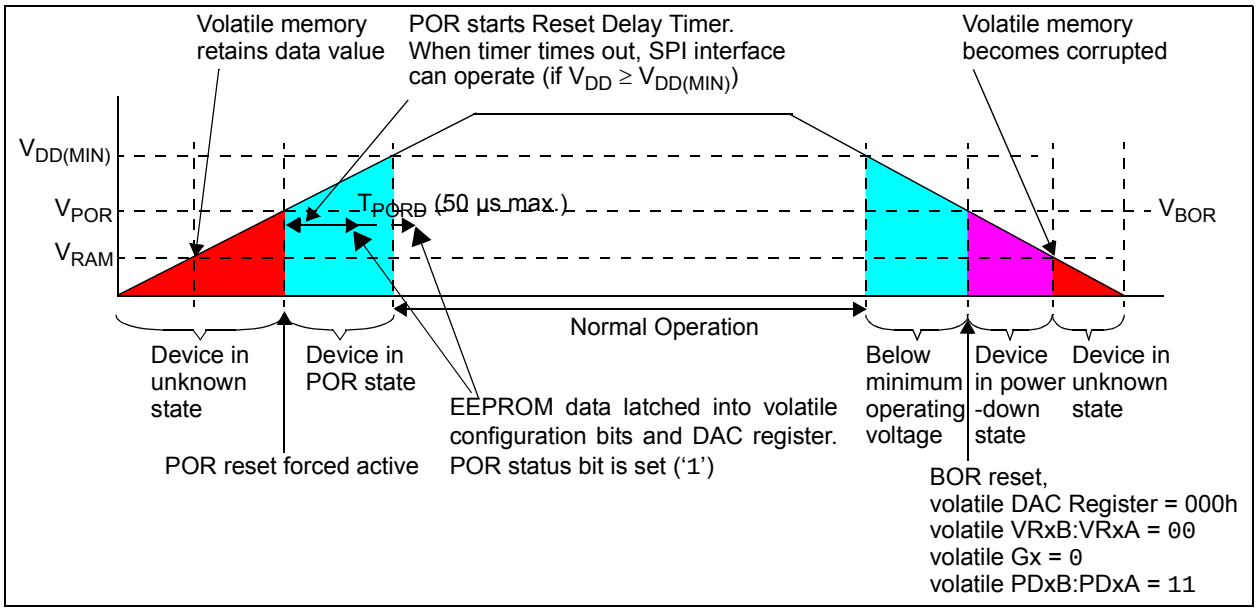


FIGURE 4-1: *Power-on Reset Operation.*

4.2 Device Memory

User memory includes three types of memory:

- **Volatile Register Memory (RAM)**
- **Nonvolatile Register Memory**
- **Device Configuration Memory**

Each memory address is 16 bits wide. There are five nonvolatile user-control bits that do not reside in memory mapped register space (see **Section 4.2.3 "Device Configuration Memory"**).

4.2.1 VOLATILE REGISTER MEMORY (RAM)

There are up to six volatile memory locations:

- DAC0 and DAC1 Output Value Registers
- VREF Select Register
- Power-Down Configuration Register
- Gain and Status Register
- WiperLock Technology Status Register

The volatile memory starts functioning when the device V_{DD} is at (or above) the RAM retention voltage (V_{RAM}). The volatile memory will be loaded with the default device values when the V_{DD} rises across the V_{POR}/V_{BOR} voltage trip point.

4.2.2 NONVOLATILE REGISTER MEMORY

This memory can be grouped into two uses of nonvolatile memory. These are the DAC Output Value and Configuration registers:

- Nonvolatile DAC0 and DAC1 Output Value Registers
- Nonvolatile VREF Select Register
- Nonvolatile Power-Down Configuration Register
- Nonvolatile Gain Register

The nonvolatile memory starts functioning below the device's V_{POR}/V_{BOR} trip point, and is loaded into the corresponding volatile registers whenever the device rises above the POR/BOR voltage trip point.

The device starts writing the EEPROM memory location at the completion of the serial interface command. For the SPI interface, this is when the $\overline{CS}$ pin goes inactive (V_{IH}).

Note:	When the nonvolatile memory is written, the corresponding volatile memory is **not** modified.

The nonvolatile DAC registers enable stand-alone operation of the device (without Microcontroller control) after being programmed to the desired value.

TABLE 4-1: MEMORY MAP (x16)

Address	Function	Config Bit (1)
00h	Volatile DAC0 Register	CL0
01h	Volatile DAC1 Register	CL1
02h	Reserved	—
03h	Reserved	—
04h	Reserved	—
05h	Reserved	—
06h	Reserved	—
07h	Reserved	—
08h	V_{REF} Register	—
09h	Power-Down Register	—
0Ah	Gain and Status Register	—
0Bh	WiperLock™ Technology Status Register	—
0Ch	Reserved	—
0Dh	Reserved	—
0Eh	Reserved	—
0Fh	Reserved	—

Address	Function	Config Bit (1)
10h	Nonvolatile DAC0 Register	DL0
11h	Nonvolatile DAC1 Register	DL1
12h	Reserved	—
13h	Reserved	—
14h	Reserved	—
15h	Reserved	—
16h	Reserved	—
17h	Reserved	—
18h	Nonvolatile V_{REF} Register	—
19h	Nonvolatile Power-Down Register	—
1Ah	NV Gain Register	—
1Bh	Reserved	—
1Ch	Reserved	—
1Dh	Reserved	—
1Eh	Reserved	—
1Fh	Reserved	—

Volatile Memory address range

Nonvolatile Memory address range

Note 1: Device Configuration Memory bits require a High-Voltage enable or disable command ($\overline{LAT}/\overline{LAT0} = V_{IHH}$, or $\overline{CS} = V_{IHH}$) to modify the bit value.

4.2.3 DEVICE CONFIGURATION MEMORY

There are up to five nonvolatile user bits that are not directly mapped into the address space. These nonvolatile device configuration bits control the following functions:

- DAC Register
- Configuration WiperLock Technology (2 bits per DAC)

The Status register shows the states of the device WiperLock Technology configuration bits. The Status register is described in Register 4-6.

The operation of WiperLock Technology is discussed in **Section 4.2.6 "WiperLock Technology"**.

4.2.4 UNIMPLEMENTED REGISTER BITS

Read commands of a valid location will read unimplemented bits as '0'.

4.2.5 UNIMPLEMENTED (RESERVED) LOCATIONS

Normal (voltage) commands (read or write) to any unimplemented memory address (reserved) will result in a command error condition (CMDERR). Read commands of a reserved location will read bits as '1'.

High-Voltage commands (enable or disable) to any unimplemented configuration bits will result in a command error condition (CMDERR).

4.2.5.1 Default Factory POR Memory State of Nonvolatile Memory (EEPROM)

Table 4-2 shows the default factory POR initialization of the device memory map for the 8-, 10- and 12-bit devices.

Note:	The volatile memory locations will be determined by the nonvolatile memory states (registers and device configuration bits).

TABLE 4-2: FACTORY DEFAULT POR / BOR VALUES

Address	Function	POR/BOR Value			Address	Function	POR/BOR Value		
		8-bit	10-bit	12-bit			8-bit	10-bit	12-bit
00h	Volatile DAC0 Register	7Fh	1FFh	7FFh	10h	Nonvolatile DAC0 Register	7Fh	1FFh	7FFh
01h	Volatile DAC1 Register	7Fh	1FFh	7FFh	11h	Nonvolatile DAC1 Register	7Fh	1FFh	7FFh
02h	Reserved (1)	FFh	3FFh	FFFh	12h	Reserved (1)	FFh	3FFh	FFFh
03h	Reserved (1)	FFh	3FFh	FFFh	13h	Reserved (1)	FFh	3FFh	FFFh
04h	Reserved (1)	FFh	3FFh	FFFh	14h	Reserved (1)	FFh	3FFh	FFFh
05h	Reserved (1)	FFh	3FFh	FFFh	15h	Reserved (1)	FFh	3FFh	FFFh
06h	Reserved (1)	FFh	3FFh	FFFh	16h	Reserved (1)	FFh	3FFh	FFFh
07h	Reserved (1)	FFh	3FFh	FFFh	17h	Reserved (1)	FFh	3FFh	FFFh
08h	V_{REF} Register	0000h	0000h	0000h	18h	Nonvolatile V_{REF} Register	0000h	0000h	0000h
09h	Power-Down Register	0000h	0000h	0000h	19h	Nonvolatile Power-Down Register	0000h	0000h	0000h
0Ah	Gain and Status Register	0080h	0080h	0080h	1Ah	NV Gain	0000h	0000h	0000h
0Bh	WiperLock™ Technology Status Register	0000h	0000h	0000h	1Bh	Reserved (1)	FFh	3FFh	FFFh
0Ch	Reserved (1)	FFh	3FFh	FFFh	1Ch	Reserved (1)	FFh	3FFh	FFFh
0Dh	Reserved (1)	FFh	3FFh	FFFh	1Dh	Reserved (1)	FFh	3FFh	FFFh
0Eh	Reserved (1)	FFh	3FFh	FFFh	1Eh	Reserved (1)	FFh	3FFh	FFFh
0Fh	Reserved (1)	FFh	3FFh	FFFh	1Fh	Reserved (1)	FFh	3FFh	FFFh

Volatile Memory address range

Nonvolatile Memory address range

Note 1: Reading a reserved memory location will result in the SPI command Command Error condition. The SDO pin will output all '0's. Forcing the $\overline{CS}$ pin to the V_{IH} state will reset the SPI interface.

4.2.6 WIPERLOCK TECHNOLOGY

The MCP48FEBXX device's WiperLock technology allows application-specific device settings (DAC register and configuration) to be secured without requiring the use of an additional write-protect pin. There are two configuration bits (DLx:CLx) for each DAC (DAC0 and DAC1).

Dependent on the state of the DLx:CLx configuration bits, WiperLock technology prevents the serial commands from the following actions on the DACx registers and bits:

- Writing to the specified volatile DACx Register memory location
- Writing to the specified nonvolatile DACx Register memory location
- Writing to the specified volatile DACx configuration bits
- Writing to the specified nonvolatile DACx configuration bits

Each pair of these configuration bits control one of four modes. These modes are shown in Table 4-3. The addresses for the configuration bits are shown in Table 4-1.

To modify the configuration bits, the HVC pin must be forced to the V_{IHH} state and then receive an enable or disable command on the desired pair of DAC Register addresses.

Note: To modify the CL0 bit, the enable or disable command specifies address 00h, while to modify the DL0 bit, the enable or disable command specifies address 10h.

Please refer to **Section 7.4 "Enable Configuration Bit"** and **Section 7.5 "Disable Configuration Bit"** commands for operation.

Note: During device communication, if the Device Address/Command combination is invalid or an unimplemented Address is specified, then the MCP48FEBXX will Command Error that Command byte. To reset the serial interface state machine, the $\overline{CS}$ pin must be driven to the inactive state (V_{IH}) before returning to the active state (V_{IL} or V_{IHH}).

4.2.6.1 POR/BOR Operation with WiperLock Technology Enabled

The WiperLock Technology state is not affected by a POR/BOR event. A POR/BOR event will load the Volatile DAC0 (DAC1) register values with the Nonvolatile DAC0 (DAC1) register values.

TABLE 4-3: WIPERLOCK™ TECHNOLOGY CONFIGURATION BITS - FUNCTIONAL DESCRIPTION

DLx:CLx (1)	Register / Bits				Comments
	DACx		DACx Configuration (2)		
	Volatile	Nonvolatile	Volatile	Nonvolatile	
11	Locked	Locked	Locked	Locked	All DACx registers are locked.
10	Locked	Locked	Unlocked	Locked	All DACx registers are locked except volatile DACx Configuration registers. This allows operation of power-down modes.
01	Unlocked	Locked	Unlocked	Locked	Volatile DACx registers unlocked, nonvolatile DACx registers locked.
00	Unlocked	Unlocked	Unlocked	Unlocked	All DACx registers are unlocked.

Note 1: The state of these configuration bits (DLx:CLx) are reflected in WLxB:WLxA bits as shown in Register 4-6.

2: DAC configuration bits include Voltage Reference Control bits (VRxB:VRxA), Power-Down Control bits (PDxB:PDxA), and Output Gain bits (Gx).

4.2.7 DEVICE REGISTERS

Register 4-1 shows the format of the DAC Output Value registers for both the volatile memory locations and the nonvolatile memory locations. These registers will be either 8 bits, 10 bits, or 12 bits wide. The values are right justified.

REGISTER 4-1: DAC0 AND DAC1 REGISTERS (VOLATILE AND NONVOLATILE)

	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
12-bit	—	—	—	—	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
10-bit	—	—	—	—	—(1)	—(1)	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
8-bit	—	—	—	—	—(1)	—(1)	—(1)	—(1)	D07	D06	D05	D04	D03	D02	D01	D00
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= 12-bit device	= 10-bit device	= 8-bit device	

12-bit	10-bit	8-bit	
bit 15-12	bit 15-10	bit 15-8	**Unimplemented:** Read as '0'
bit 11-0	—	—	**D11-D00:** DAC Output value - 12-bit devices FFFh = Full-Scale output value 7FFh = Mid-Scale output value 000h = Zero-Scale output value
—	bit 9-0	—	**D09-D00:** DAC Output value - 10-bit devices 3FFh = Full-Scale output value 1FFh = Mid-Scale output value 000h = Zero-Scale output value
—	—	bit 7-0	**D07-D00:** DAC Output value - 8-bit devices FFh = Full-Scale output value 7Fh = Mid-Scale output value 000h = Zero-Scale output value

Note 1: Unimplemented bit, read as '0'.

Register 4-2 shows the format of the Voltage Reference Control Register. Each DAC has two bits to control the source of the voltage reference of the DAC. This register is for both the volatile memory locations and the nonvolatile memory locations.

REGISTER 4-2: VOLTAGE REFERENCE (VREF) CONTROL REGISTER (VOLATILE AND NONVOLATILE) (ADDRESSES 08h AND 18h)

	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
Single	—	—	—	—	—	—	—	—	—	—	—	—	—(1)	—(1)	VR0B	VR0A
Dual	—	—	—	—	—	—	—	—	—	—	—	—	VR1B	VR1A	VR0B	VR0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Single-channel device		= Dual-channel device	

Single	Dual	
bit 15-2	bit 15-4	**Unimplemented:** Read as '0'
bit 1-0	bit 3-0	**VRxB-VRxA:** DAC Voltage Reference Control bits 11 = V_{REF} pin (Buffered); V_{REF} buffer enabled 10 = V_{REF} pin (Unbuffered); V_{REF} buffer disabled 01 = Internal Band Gap (1.22V typical); V_{REF} buffer enabled V_{REF} voltage driven when powered-down 00 = V_{DD} (Unbuffered); V_{REF} buffer disabled. Use this state with Power-Down bits for lowest current.

Note 1: Unimplemented bit, read as '0'.

Register 4-3 shows the format of the Power-Down Control Register. Each DAC has two bits to control the Power-Down state of the DAC. This register is for both the volatile memory locations and the nonvolatile memory locations.

REGISTER 4-3: POWER-DOWN CONTROL REGISTER (VOLATILE AND NONVOLATILE) (ADDRESSES 09h, 19h)

	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
Single	—	—	—	—	—	—	—	—	—	—	—	—	—(1)	—(1)	PD0B	PD0A
Dual	—	—	—	—	—	—	—	—	—	—	—	—	PD1B	PD1A	PD0B	PD0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Single-channel device		= Dual-channel device	

Single	Dual	
bit 15-2	bit 15-4	**Unimplemented:** Read as '0'
bit 1-0	bit 3-0	**PDxB-PDxA:** DAC Power-Down Control bits(2) 11 = Powered Down - V_{OUT} is open circuit. 10 = Powered Down - V_{OUT} is loaded with a 100 kΩ resistor to ground. 01 = Powered Down - V_{OUT} is loaded with a 1 kΩ resistor to ground. 00 = Normal Operation (Not powered-down)

Note 1: Unimplemented bit, read as '0'.

2: See Table 5-5 and Figure 5-10 for more details.

Register 4-4 shows the format of the volatile Gain Control and System Status Register. Each DAC has one bit to control the gain of the DAC and three Status bits.

REGISTER 4-4: GAIN CONTROL AND SYSTEM STATUS REGISTER (VOLATILE) (ADDRESS 0Ah)

	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/C-1	R-0	U-0	U-0	U-0	U-0	U-0	U-0
Single	—	—	—	—	—	—	—(1)	G0	POR	EEWA	—	—	—	—	—	—
Dual	—	—	—	—	—	—	G1	G0	POR	EEWA	—	—	—	—	—	—
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clear-able bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Single-channel device		= Dual-channel device	

Single	Dual	
bit 15-9	bit 15-10	**Unimplemented:** Read as '0'
—	bit 9	**G1:** DAC1 Output Driver Gain control bits (**Dual-Channel Device only**) 1 = 2x Gain 0 = 1x Gain
bit 8	bit 8	**G0:** DAC0 Output Driver Gain control bits 1 = 2x Gain 0 = 1x Gain
bit 7	bit 7	**POR:** Power-on Reset (Brown-out Reset) Status bit This bit indicates if a Power-on Reset (POR) or Brown-out Reset (BOR) event has occurred since the last read command of this register. Reading this register clears the state of the POR Status bit. 1 = A POR (BOR) event occurred since the last read of this register. Reading this register clears this bit. 0 = A POR (BOR) event has not occurred since the last read of this register.
bit 6	bit 6	**EEWA:** EEPROM Write Active Status bit This bit indicates if the EEPROM Write Cycle is occurring. 1 = An EEPROM Write Cycle is currently occurring. Only serial commands to the volatile memory are allowed. 0 = An EEPROM Write Cycle is NOT currently occurring.
bit 5-0	bit 5-0	**Unimplemented:** Read as '0'

Note 1: Unimplemented bit, read as '0'.

Register 4-5 shows the format of the Nonvolatile Gain Control Register. Each DAC has one bit to control the gain of the DAC.

REGISTER 4-5: GAIN CONTROL REGISTER (NONVOLATILE) (ADDRESS 1Ah)

	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
Single	—	—	—	—	—	—	—(1)	G0	—	—	—	—	—	—	—	—
Dual	—	—	—	—	—	—	G1	G0	—	—	—	—	—	—	—	—
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Single-channel device		= Dual-channel device	

Single	Dual	
bit 15-9	bit 15-10	**Unimplemented:** Read as '0'
—	bit 9	**G1:** DAC1 Output Driver Gain control bits (**Dual-Channel Device only**) 1 = 2x Gain 0 = 1x Gain
bit 8	bit 8	**G0:** DAC0 Output Driver Gain control bits 1 = 2x Gain 0 = 1x Gain
bit 7-0	bit 6-0	**Unimplemented:** Read as '0'

Note 1: Unimplemented bit, read as '0'.

Register 4-6 shows the format of the DAC WiperLock Technology Status Register.

REGISTER 4-6: DAC WIPERLOCK TECHNOLOGY STATUS REGISTER (VOLATILE) (ADDRESS 0BH)

	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0(1)	R-0(1)	R-0(1)	R-0(1)
Single	—	—	—	—	—	—	—	—	—	—	—	—	—(2)	—(2)	WL0B	WL0A
Dual	—	—	—	—	—	—	—	—	—	—	—	—	WL1B	WL1A	WL0B	WL0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Single-channel device		= Dual-channel device	

Single	Dual	
bit 15-2	bit 15-4	**Unimplemented:** Read as '0'
bit 1-0	bit 3-0	**WLxB-WLxA:** WiperLock Technology Status bits: These bits reflect the state of the DLx:CLx nonvolatile configuration bits. 11 = DAC wiper and DAC Configuration (volatile and nonvolatile registers) are locked. (DLx = CLx = Enabled) 10 = DAC wiper (volatile and nonvolatile) and DAC Configuration (nonvolatile registers) are locked (DLx = Enabled; CLx = Disabled). 01 = DAC wiper (nonvolatile) and DAC Configuration (nonvolatile registers) are locked. (DLx = Disabled; CLx = Enabled) 00 = DAC wiper and DAC Configuration are unlocked (DLx = CLx = Disabled).

Note 1: POR Value dependent on the programmed values of the DLx:CLx configuration bits. The devices are shipped with a default DLx:CLx configuration bit state of '0'.

2: Unimplemented bit, read as '0'.

NOTES:

5.0 DAC CIRCUITRY

The Digital-to-Analog Converter circuitry converts a digital value into its analog representation. The description details the functional operation of the device.

The DAC Circuit uses a resistor ladder implementation. Devices have up to two DACs.

Figure 5-1 shows the functional block diagram for the MCP48FEBXX DAC circuitry.

The functional blocks of the DAC include:

- **Resistor Ladder**
- **Voltage Reference Selection**
- **Output Buffer/V_{OUT} Operation**
- **Internal Band Gap** (as a voltage reference)
- **Latch Pin (LAT)**
- **Power-Down Operation**

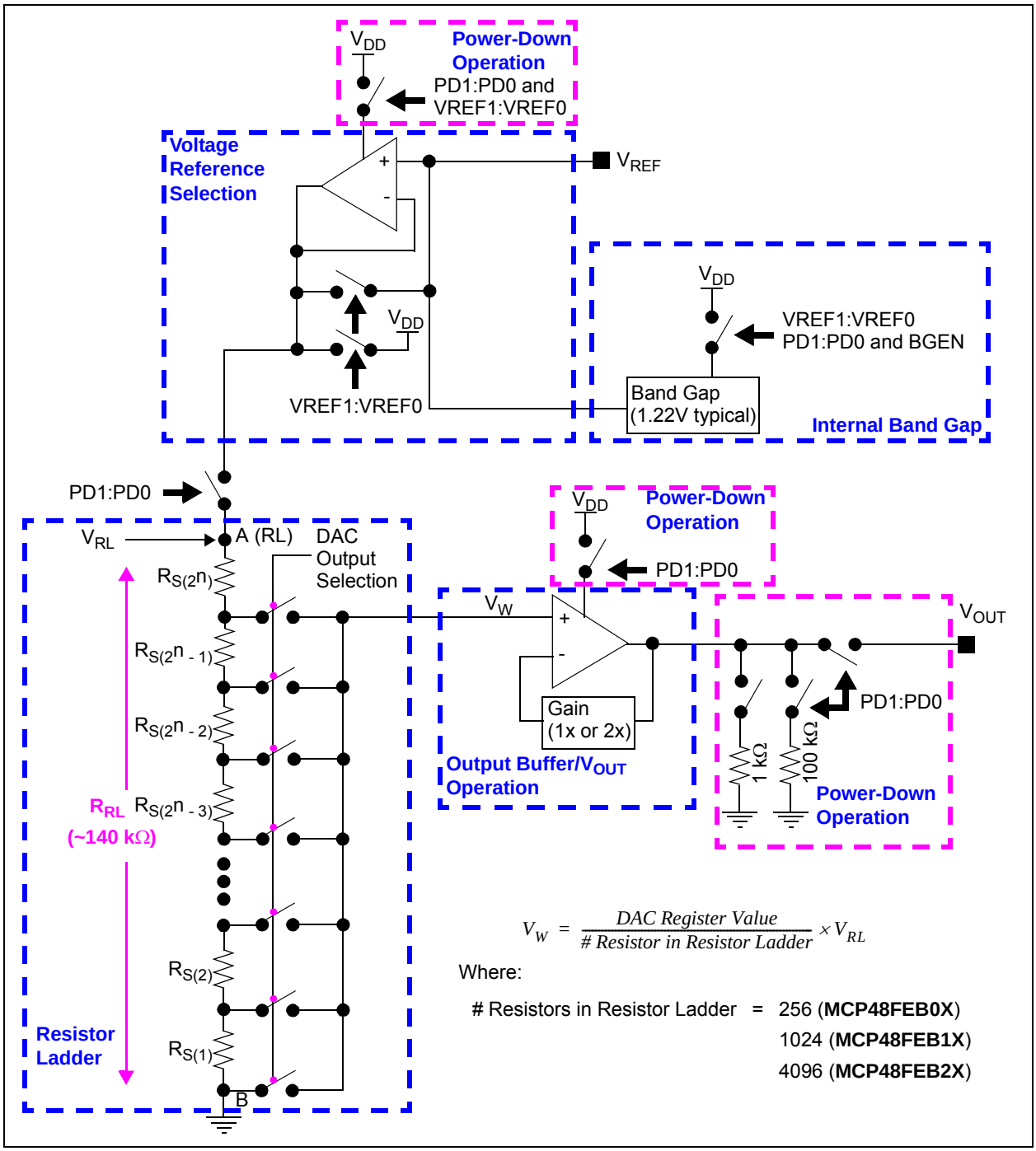


FIGURE 5-1: *MCP48FEBXX DAC Module Block Diagram.*

5.1 Resistor Ladder

The Resistor Ladder is a digital potentiometer with the B terminal internally grounded and the A terminal connected to the selected reference voltage (see Figure 5-2). The volatile DAC register controls the wiper position. The wiper voltage (V_W) is proportional to the DAC register value divided by the number of resistor elements (R_S) in the ladder (256, 1024 or 4096) related to the V_{RL} voltage.

The output of the resistor network will drive the input of an output buffer.

The Resistor Network is made up of these three parts:

- Resistor Ladder (string of R_S elements)
- Wiper switches
- DAC Register decode

The resistor ladder (R_{RL}) has a typical impedance of approximately 140 kΩ. This resistor ladder resistance (R_{RL}) may vary from device to device by up to ±20%. Since this is a voltage divider configuration, the actual R_{RL} resistance does not affect the output given a fixed voltage at V_{RL}.

Equation 5-1 shows the calculation for the step resistance:

EQUATION 5-1: R_S CALCULATION

$$R_S = \frac{R_{RL}}{(256)} \quad \text{8-bit Device}$$

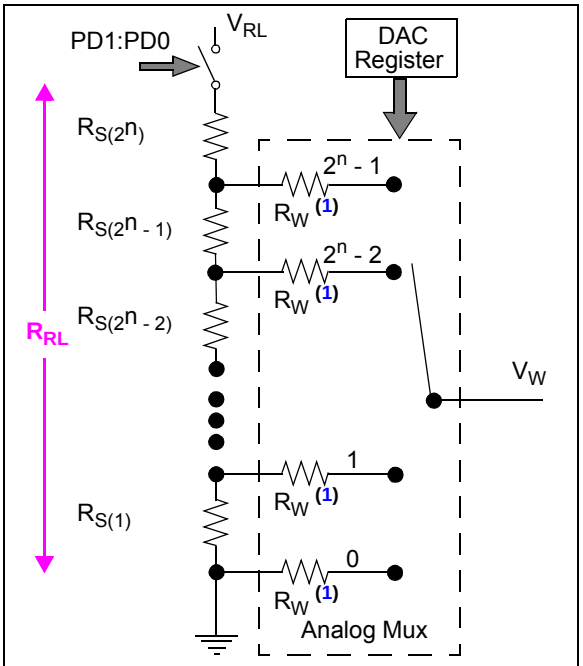
$$R_S = \frac{R_{RL}}{(1024)} \quad \text{10-bit Device}$$

$$R_S = \frac{R_{RL}}{(4096)} \quad \text{12-bit Device}$$

Note: The maximum wiper position is $2^n - 1$, while the number of resistors in the resistor ladder is 2^n. This means that when the DAC register is at full-scale, there is one resistor element (R_S) between the wiper and the V_{RL} voltage.

If the unbuffered V_{REF} pin is used as the V_{RL} voltage source, this voltage source should have a low output impedance.

When the DAC is powered-down, the resistor ladder is disconnected from the selected reference voltage.



$$V_W = \frac{DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times V_{RL}$$

Where:

Resistors in R-Ladder = 256 (**MCP48FEB0X**)
1024 (**MCP48FEB1X**)
4096 (**MCP48FEB2X**)

Note 1: The analog switch resistance (R_W) does not affect performance due to the voltage divider configuration.

FIGURE 5-2: *Resistor Ladder Model Block Diagram.*

5.2 Voltage Reference Selection

The resistor ladder has up to four sources for the reference voltage. Two user control bits (VREF1:VREF0) are used to control the selection, with the selection connected to the V_{RL} node (see Figures 5-3 and 5-4). The four voltage source options for the Resistor Ladder are:

1. V_{DD} pin voltage
2. Internal Voltage Reference (V_{BG})
3. V_{REF} pin voltage unbuffered
4. V_{REF} pin voltage internally buffered

The selection of the voltage is specified with the volatile V_{REF1}:V_{REF0} configuration bits (see Register 4-2). There are nonvolatile and volatile VREF1:VREF0 configuration bits. On a POR/BOR event, the state of the nonvolatile VREF1:VREF0 configuration bits is latched into the volatile VREF1:VREF0 configuration bits.

When the user selects the V_{DD} as reference, the V_{REF} pin voltage is not connected to the resistor ladder.

If the V_{REF} pin is selected, then a selection has to be made between the Buffered or Unbuffered mode.

5.2.1 UNBUFFERED MODE

The V_{REF} pin voltage may be from V_{SS} to V_{DD}.

Note 1:	The voltage source should have a low output impedance. If the voltage source has a high output impedance, then the voltage on the V_{REF}'s pin would be lower than expected. The resistor ladder has a typical impedance of 140 kΩ and a typical capacitance of 29 pF.
2:	If the V_{REF} pin is tied to the V_{DD} voltage, V_{DD} mode (VREF1:VREF0 = '00') is recommended.

5.2.2 BUFFERED MODE

The V_{REF} pin voltage may be from 0.01V to V_{DD} - 0.04V. The input buffer (amplifier) provides low offset voltage, low noise, and a very high input impedance, with only minor limitations on the input range and frequency response.

Note 1:	Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.
2:	If the V_{REF} pin is tied to the V_{DD} voltage, V_{DD} mode (VREF1:VREF0 = '00') is recommended.

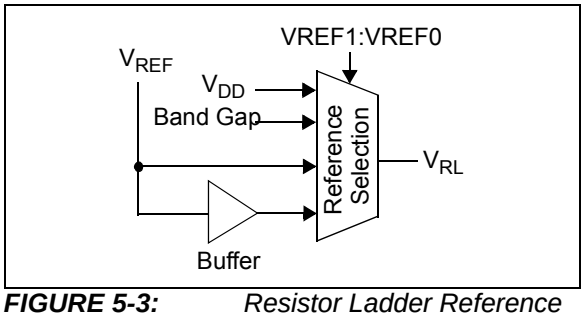
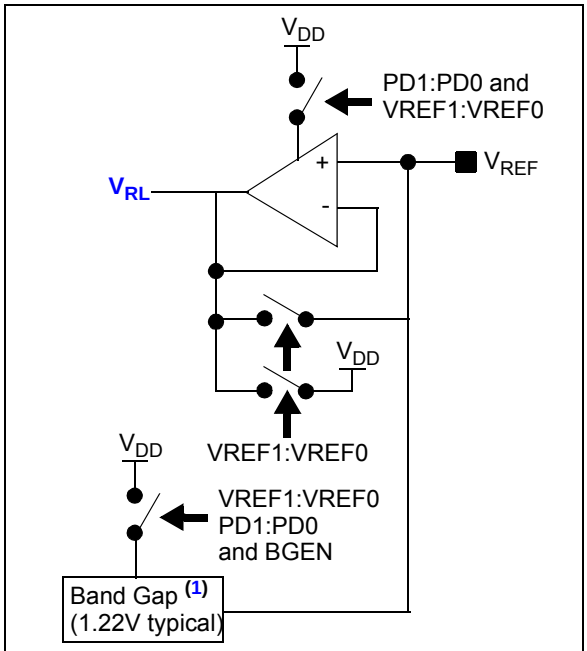


FIGURE 5-3: *Resistor Ladder Reference Voltage Selection Block Diagram.*



Note 1: The Band Gap voltage (V_{BG}) is 1.22V typical. The band gap output goes through the buffer with a 2x gain to create the V_{RL} voltage. See **Section 5.4 "Internal Band Gap"** for additional information on the band gap circuit.

FIGURE 5-4: *Reference Voltage Selection Implementation Block Diagram.*

5.2.3 BAND GAP MODE

If the Internal Band Gap is selected, then the external V_{REF} pin should not be driven and only use high-impedance loads. Decoupling capacitors are recommended for optimal operation.

The band gap output is buffered, but the internal switches limit the current that the output should source to the V_{REF} pin. The resistor ladder buffer is used to drive the Band Gap voltage for the cases of multiple DAC outputs. This ensures that the resistor ladders are always properly sourced when the band gap is selected.

5.3 Output Buffer/V_{OUT} Operation

The Output Driver buffers the wiper voltage (V_W) of the Resistor Ladder.

The DAC output is buffered with a low power and precision output amplifier (op amp). This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier's output can drive the resistive and high-capacitive loads without oscillation. The amplifier provides a maximum load current which is enough for most programmable voltage reference applications. Refer to **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.

Note:	The load resistance must keep higher than 5 kΩ for the stable and expected analog output (to meet electrical specifications).

Figure 5-5 shows the block diagram of the output driver circuit.

The user can select the output gain of the output amplifier. The gain options are:

a) Gain of 1, with either the V_{DD} or V_{REF} pin used as reference voltage.

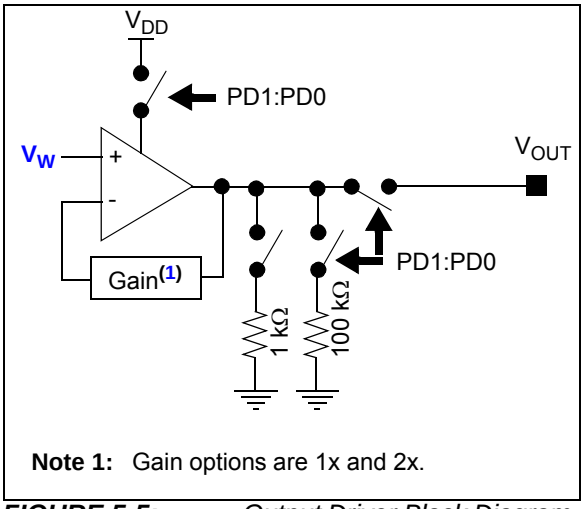
b) Gain of 2.

Power-down logic also controls the output buffer operation (see **Section 5.6 "Power-Down Operation"** for additional information on Power-Down). In any of the three power-down modes, the op amp is powered-down and its output becomes a high impedance to the V_{OUT} pin.

Table 5-1 shows the gain bit operation.

TABLE 5-1: OUTPUT DRIVER GAIN

Gain Bit	Gain	Comment
0	1	
1	2	Limits V_{REF} pin voltages relative to device V_{DD} voltage.



Note 1: Gain options are 1x and 2x.

FIGURE 5-5: *Output Driver Block Diagram.*

5.3.1 PROGRAMMABLE GAIN

The amplifier's gain is controlled by the Gain (G) configuration bit (see Register 4-5) and the V_{RL} reference selection.

The volatile G bit value can be modified by:

- POR events
- BOR events
- SPI write commands

5.3.2 OUTPUT VOLTAGE

The volatile DAC Register values, along with the device's configuration bits, control the analog V_{OUT} voltage. The volatile DAC Register's value is unsigned binary. The formula for the output voltage is given in Equation 5-2. Table 5-3 shows examples of volatile DAC register values and the corresponding theoretical V_{OUT} voltage for the MCP48FEBXX devices.

EQUATION 5-2: CALCULATING OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{V_{RL} \times DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

Resistors in R-Ladder = 4096 (**MCP48FEB2X**)
1024 (**MCP48FEB1X**)
256 (**MCP48FEB0X**)

Note: When Gain = 2 ($V_{RL} = V_{REF}$) and if $V_{REF} > V_{DD} / 2$, the V_{OUT} voltage will be limited to V_{DD}. So if $V_{REF} = V_{DD}$, then the V_{OUT} voltage will not change for volatile DAC Register values mid-scale and greater, since the op amp is at full-scale output.

The following events update the DAC register value and therefore the analog voltage output (V_{OUT}):

- Power-on Reset
- Brown-out Reset
- `Write` command

The V_{OUT} voltage will start driving to the new value after the event has occurred.

5.3.3 STEP VOLTAGE (V_S)

The Step Voltage is dependent on the device resolution and the calculated output voltage range. One LSb is defined as the ideal voltage difference between two successive codes. The step voltage can easily be calculated by using Equation 5-3 (DAC Register Value is equal to 1). Theoretical step voltages are shown in Table 5-2 for several V_{REF} voltages.

EQUATION 5-3: V_S CALCULATION

$$V_S = \frac{V_{RL}}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

Resistors in R-Ladder = 4096 (**12-bit**)
1024 (**10-bit**)
256 (**8-bit**)

TABLE 5-2: THEORETICAL STEP VOLTAGE (V_S) (1)

	V_{REF}					
	5.0	**2.7**	**1.8**	**1.5**	**1.0**	
V_S	1.22 mV	659 uV	439 uV	366 uV	244 uV	12-bit
	4.88 mV	2.64 mV	1.76 mV	1.46 mV	977 uV	10-bit
	19.5 mV	10.5 mV	7.03 mV	5.86 mV	3.91 mV	8-bit

Note 1: When Gain = 1x, $V_{FS} = V_{RL}$, and $V_{ZS} = 0V$.

5.3.4 OUTPUT SLEW RATE

Figure 5-6 shows an example of the slew rate of the V_{OUT} pin. The slew rate can be affected by the characteristics of the circuit connected to the V_{OUT} pin.

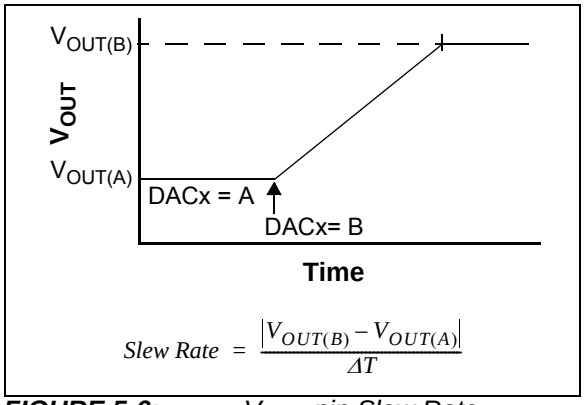


FIGURE 5-6: *V_{OUT} pin Slew Rate.*

5.3.4.1 Small Capacitive Load

With a small capacitive load, the output buffer's current is not affected by the capacitive load (C_L). But still, the V_{OUT} pin's voltage is not a step transition from one output value (DAC register value) to the next output value. The change of the V_{OUT} voltage is limited by the output buffer's characteristics, so the V_{OUT} pin voltage will have a slope from the old voltage to the new voltage. This slope is fixed for the output buffer, and is referred to as the buffer slew rate (SR_{BUF}).

5.3.4.2 Large Capacitive Load

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer's short-circuit current (I_{SC})
- The V_{OUT} pin's external load

I_{OUT} cannot exceed the output buffer's short-circuit current (I_{SC}), which fixes the output buffer slew rate (SR_{BUF}). The voltage on the capacitive load (C_L), V_{CL}, changes at a rate proportional to I_{OUT}, which fixes a capacitive load slew rate (SR_{CL}).

The V_{CL} voltage slew rate is limited to the slower of the output buffer's internally set slew rate (SRBUF) and the capacitive load slew rate (SR_{CL}).

5.3.5 DRIVING RESISTIVE AND CAPACITIVE LOADS

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications). A V_{OUT} vs. Resistive Load characterization graph is provided in the Typical Performance Curves for this device (**DS20005440**).

V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended to use a load with R_L greater than 5 kΩ.

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the V_{OUT} pin's voltage does not quickly follow the buffer's input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the V_{OUT} pin.

When driving large capacitive loads with the output buffer, a small series resistor (R_{ISO}) at the output (see Figure 5-7) improves the output buffer's stability (feedback loop's phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

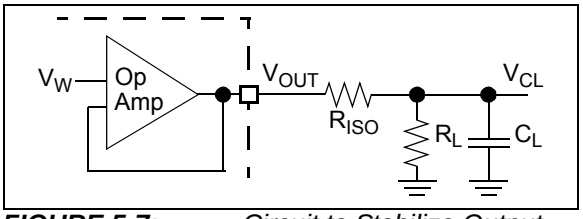


FIGURE 5-7: *Circuit to Stabilize Output Buffer for Large Capacitive Loads (C_L).*

The R_{ISO} resistor value for your circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this R_{ISO} resistor value should be verified on the bench. Modify the R_{ISO}'s resistance value until the output characteristics meet your requirements.

A method to evaluate the system's performance is to inject a step voltage on the V_{REF} pin and observe the V_{OUT} pin's characteristics.

Note:	Additional insight into circuit design for driving capacitive loads can be found in AN884 – *"Driving Capacitive Loads With Op Amps"* (DS00884).

TABLE 5-3: DAC INPUT CODE VS. CALCULATED ANALOG OUTPUT (V_{OUT}) (V_{DD} = 5.0V)

Device	Volatile DAC Register Value	V_{RL} (1)	LSb		Gain Selection (2)	V_{OUT} (3)	
			Equation	µV		Equation	V
MCP48FEB2X (12-bit)	1111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (4095/4096) * 1$	4.998779
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (4095/4096) * 1$	2.499390
					2x(2)	$V_{RL} * (4095/4096) * 2)$	4.998779
	0111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (2047/4096) * 1)$	2.498779
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (2047/4096) * 1)$	1.249390
					2x(2)	$V_{RL} * (2047/4096) * 2)$	2.498779
	0011 1111 1111	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (1023/4096) * 1)$	1.248779
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (1023/4096) * 1)$	0.624390
					2x(2)	$V_{RL} * (1023/4096) * 2)$	1.248779
	0000 0000 0000	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (0/4096) * 1)$	0
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (0/4096) * 1)$	0
					2x(2)	$V_{RL} * (0/4096) * 2)$	0
MCP48FEB1X (10-bit)	11 1111 1111	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (1023/1024) * 1$	4.995117
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (1023/1024) * 1$	2.497559
					2x(2)	$V_{RL} * (1023/1024) * 2$	4.995117
	01 1111 1111	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (511/1024) * 1$	2.495117
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (511/1024) * 1$	1.247559
					2x(2)	$V_{RL} * (511/1024) * 2$	2.495117
	00 1111 1111	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (255/1024) * 1$	1.245117
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (255/1024) * 1$	0.622559
					2x(2)	$V_{RL} * (255/1024) * 2$	1.245117
	00 0000 0000	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (0/1024) * 1$	0
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (0/1024) * 1$	0
					2x(2)	$V_{RL} * (0/1024) * 1$	0
MCP48FEB0X (8-bit)	1111 1111	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (255/256) * 1$	4.980469
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (255/256) * 1$	2.490234
					2x(2)	$V_{RL} * (255/256) * 2$	4.980469
	0111 1111	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (127/256) * 1$	2.480469
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (127/256) * 1$	1.240234
					2x(2)	$V_{RL} * (127/256) * 2$	2.480469
	0011 1111	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (63/256) * 1$	1.230469
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (63/256) * 1$	0.615234
					2x(2)	$V_{RL} * (63/256) * 2$	1.230469
	0000 0000	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (0/256) * 1$	0
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (0/256) * 1$	0
					2x(2)	$V_{RL} * (0/256) * 2$	0

Note 1: V_{RL} is the resistor ladder's reference voltage. It is independent of VREF1:VREF0 selection.

2: Gain selection of 2x (Gx = '1') requires voltage reference source to come from V_{REF} pin (VREF1:VREF0 = '10' or '11') and requires V_{REF} pin voltage (or V_{RL}) ≤ $V_{DD}/2$, or from the internal band gap (VREF1:VREF0 = '01').

3: These theoretical calculations do not take into account the Offset, Gain and Nonlinearity errors.

5.4 Internal Band Gap

The internal band gap is designed to drive the Resistor Ladder Buffer.

The resistance of a resistor ladder (R_{RL}) is targeted to be 140 kΩ (±40 kΩ), which means a minimum resistance of 100 kΩ.

The band gap selection can be used across the V_{DD} voltages while maximizing the V_{OUT} voltage ranges. For V_{DD} voltages below the 2 ∗ Gain ∗ V_{BG} voltage, the output for the upper codes will be clipped to the V_{DD} voltage. Table 5-4 shows the maximum DAC register code given device VDD and Gain bit setting.

TABLE 5-4: V_{OUT} USING BAND GAP

V_{DD}	DAC Gain	Max DAC Code (1)			Comment
		12-bit	10-bit	8-bit	
5.5	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.44V (2)
	2	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 4.88V (2)
2.7	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.44V (2)
	2	8DAh	236h	8Dh	~ 0 to 55% range
2.0(3)	1	D1Dh	347h	D1h	~ 0 to 82% range
	2(4)	68Eh	1A3h	68h	~ 0 to 41% range

Note 1: Without the V_{OUT} pin voltage being clipped.
2: When V_{BG} = 1.22V typical.
3: Band gap performance achieves full performance starting from a V_{DD} of 2.0V.
4: It is recommended to use Gain = 1 setting instead.

5.5 Latch Pin ($\overline{LAT}$)

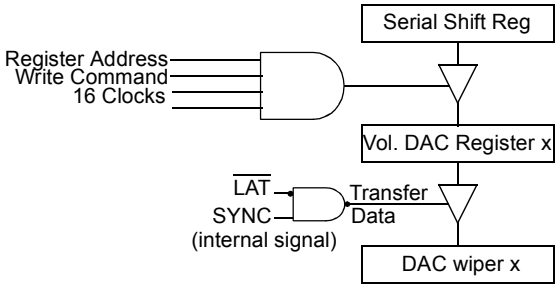
The Latch pin controls when the volatile DAC Register value is transferred to the DAC wiper. This is useful for applications that need to synchronize the wiper(s) updates to an external event, such as zero crossing or updates to the other wipers on the device. The $\overline{LAT}$ pin is asynchronous to the serial interface operation.

When the $\overline{LAT}$ pin is high, transfers from the volatile DAC register to the DAC wiper are inhibited. The volatile DAC register value(s) can be continued to be updated.

When the $\overline{LAT}$ pin is low, the volatile DAC register value is transferred to the DAC wiper.

Note:	This allows both the volatile DAC0 and DAC1 Registers to be updated while the $\overline{LAT}$ pin is high, and to have outputs synchronously updated as the $\overline{LAT}$ pin is driven low.

Figure 5-8 shows the interaction of the $\overline{LAT}$ pin and the loading of the DAC wiper x (from the volatile DAC Register x). The transfers are level driven. If the $\overline{LAT}$ pin is held low, the corresponding DAC wiper is updated as soon as the volatile DAC Register value is updated.



$\overline{LAT}$	SYNC	Transfer Data	Comment
1	1	0	No Transfer
1	0	0	No Transfer
0	1	1	Vol. DAC Register x → DAC wiper x
0	0	0	No Transfer

FIGURE 5-8: *LAT and DAC Interaction.*

The $\overline{LAT}$ pin allows the DAC wiper to be updated to an external event as well as have multiple DAC channels/devices update at a common event.

Since the DAC wiper x is updated from the Volatile DAC Register x, all DACs that are associated with a given $\overline{LAT}$ pin can be updated synchronously.

If the application does not require synchronization, then this signal should be tied low.

Figure 5-9 shows two cases of using the $\overline{LAT}$ pin to control when the wiper register is updated relative to the value of a sine wave signal.

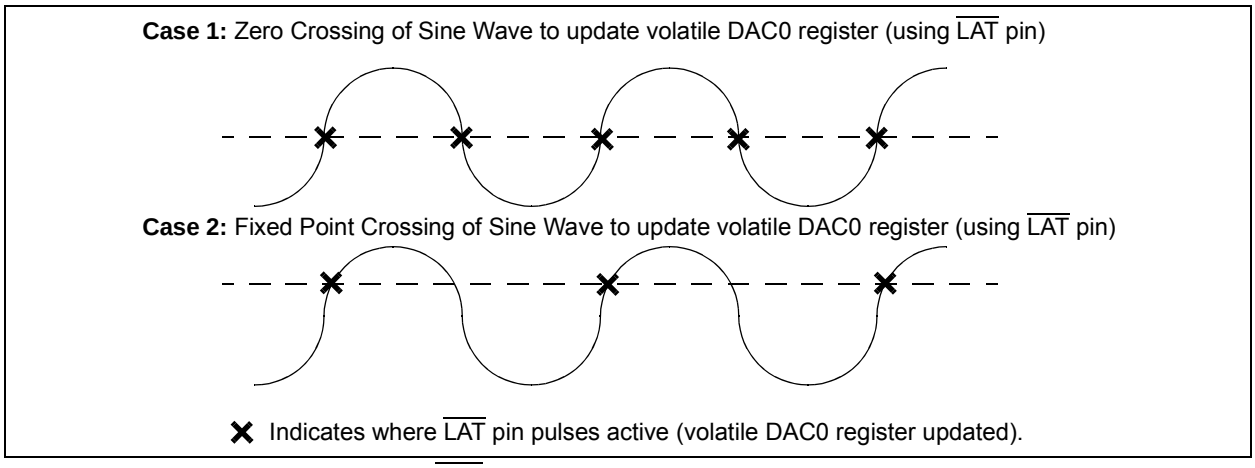


FIGURE 5-9: *Example use of $\overline{LAT}$ pin operation.*

5.6 Power-Down Operation

To allow the application to conserve power when the DAC operation is not required, three power-down modes are available. The Power-Down configuration bits (PD1:PD0) control the power-down operation (Figure 5-10 and Table 5-5). On devices with multiple DACs, each DACs power-down mode is individually controllable. All power-down modes do the following:

- Turn off most the DAC module's internal circuits (output op amp, resistor ladder, et al.)
- Op amp output becomes high-impedance to the V_{OUT} pin
- Disconnects resistor ladder from reference voltage (V_{RL})
- Retains the value of the volatile DAC register and configuration bits and the nonvolatile (EEPROM) DAC register and configuration bits

Depending on the selected power-down mode, the following will occur:

- V_{OUT} pin is switched to one of two resistive pull-downs (See Table 5-5):
  - 100 kΩ (typical)
  - 1 kΩ (typical)
- Op amp is powered-down and the V_{OUT} pin becomes high-impedance.

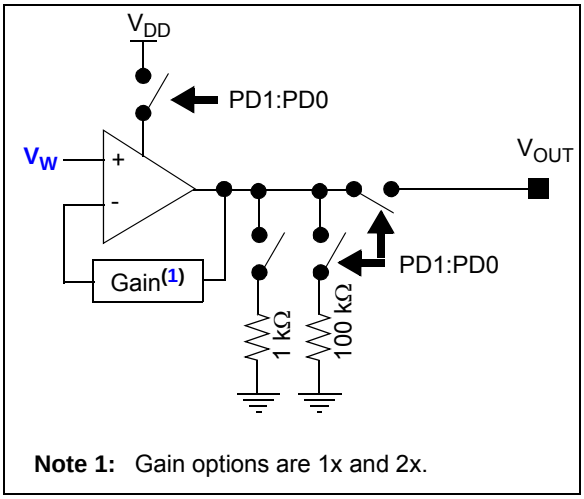
There is a delay (T_{PDE}) between the PD1:PD0 bits changing from '00' to either '01', '10' or '11' with the op amp no longer driving the V_{OUT} output and the pull-down resistors sinking current.

In any of the power-down modes where the V_{OUT} pin is not externally connected (sinking or sourcing current), the power-down current will typically be ~650 nA for a single-DAC device. As the number of DACs increases, the device's power-down current will also increase.

The Power-Down bits are modified by using a write command to the volatile Power-Down register, or a POR event which transfers the nonvolatile Power-Down register to the volatile Power-Down register.

Section 7.0 "SPI Commands" describes the SPI commands. The Write Command can be used to update the volatile PD1:PD0 bits.

Note:	The SPI serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the host controller device.



Note 1: Gain options are 1x and 2x.

FIGURE 5-10: *V_{OUT} Power-Down Block Diagram.*

TABLE 5-5: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD

PD1	PD0	Function
0	0	Normal operation
0	1	1 kΩ resistor to ground
1	0	100 kΩ resistor to ground
1	1	Open Circuit

Table 5-6 shows the current sources for the DAC based on the selected source of the DAC's reference voltage and if the device is in normal operating mode or one of the power-down modes.

TABLE 5-6: DAC CURRENT SOURCES

Device V_{DD} Current Source	PD1:0 = '00', VREF1:0 =				PD1:0 ≠ '00', VREF1:0 =			
	00	01	10	11	00	01	10	11
Output Op Amp	Y	Y	Y	Y	N	N	N	N
Resistor Ladder	Y	Y	N (1)	Y	N	N	N (1)	N
RL Op Amp	N	Y	N	Y	N	N	N	N
Band Gap	N	Y	N	N	N	Y	N	N

Note 1: Current is sourced from the V_{REF} pin, not the device V_{DD}.

5.6.1 EXITING POWER-DOWN

When the device exits Power-Down mode, the following occurs:

- Disabled circuits (op amp, resistor ladder, et al.) are turned on
- The resistor ladder is connected to selected reference voltage (V_{RL})
- The selected pull-down resistor is disconnected
- The V_{OUT} output will be driven to the voltage represented by the volatile DAC Register's value and configuration bits

The V_{OUT} output signal will require time as these circuits are powered-up and the output voltage is driven to the specified value as determined by the volatile DAC register and configuration bits.

Note:	Since the op amp and resistor ladder were powered-off (0V), the op amp's input voltage (V_W) can be considered 0V. There is a delay (T_{PDD}) between the PD1:PD0 bits updating to '00' and the op amp driving the V_{OUT} output. The op amp's settling time (from 0V) needs to be taken into account to ensure the V_{OUT} voltage reflects the selected value.

A write command forcing the PD1:PD0 bits to '00', will cause the device to exit the power-down mode.

5.7 DAC Registers, Configuration Bits, and Status Bits

The MCP48FEBXX devices have both volatile and nonvolatile (EEPROM) memory. Table 4-2 shows the volatile and non-volatile memory and their interaction due to a POR event.

There are five configuration bits in both the volatile and nonvolatile memory, the DAC registers in both the volatile and nonvolatile memory, and two volatile status bits. The DAC registers (volatile and nonvolatile) will be either 12 bits (MCP48FEB2X), 10 bits (MCP48FEB1X), or 8 bits (MCP48FEB0X) wide.

When the device is first powered-up, it automatically uploads the EEPROM memory values to the volatile memory. The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered-up, the user can update the device memory.

The SPI interface is how this memory is read and written. Refer to **Section 6.0 "SPI Serial Interface Module"** and **Section 7.0 "SPI Commands"** for more details on reading and writing the device's memory.

When the nonvolatile memory is written, the device starts writing the EEPROM cell at the rising edge of the $\overline{CS}$ pin.

Register 4-4 shows the operation of the device status bits, Table 4-1 and Table 4-3 show the operation of the device configuration bits, and Table 4-2 shows the factory default value of a POR/BOR event for the device configuration bits.

There are two status bits. These are only in volatile memory and give indication on the status of the device. The POR bit indicates if the device V_{DD} is above or below the POR trip point. During normal operation, this bit should be '1'. The EEWA bit indicates if an EEPROM write cycle is in progress. While the EEWA bit is low (during the EEPROM writing), all commands are ignored, except for the Read command.

NOTES:

6.0 SPI SERIAL INTERFACE MODULE

The MCP48FEBXX's SPI Serial Interface Module supports the SPI serial protocol specification. Figure 6-1 shows a typical SPI interface connection.

The command format and waveforms for the MCP48FEBXX is defined in **Section 7.0 "SPI Commands"**.

6.1 Overview

This sections discusses some of the specific characteristics of the MCP48FEBXX's Serial Interface Module.

The following sections discuss some of these device-specific characteristics:

- **Communication Data Rates**
- **Communication Data Rates**
- **POR/BOR**
- **Interface Pins (CS, SCK, SDI, SDO, and LAT/HVC)**

6.2 SPI SERIAL INTERFACE

The MCP48FEBXX devices support the SPI serial protocol. This SPI operates in slave mode (does not generate the serial clock).

The SPI interface uses up to four pins. These are:

- $\overline{CS}$ - Chip Select
- SCK - Serial Clock
- SDI - Serial Data In
- SDO - Serial Data Out

An additional HVC pin is available for High Voltage command support. High Voltage commands allow the device to enable and disable nonvolatile configuration bits. Without high voltage present, those bits are inhibited from being modified.

Typical SPI Interfaces are shown in Figure 6-1. In the SPI interface, the Master's Output pin is connected to the Slave's Input pin, and the Master's Input pin is connected to the Slave's Output pin.

The MCP48FEBXX SPI's module supports two (of the four) standard SPI modes. These are Mode `0,0` and `1,1`. The SPI mode is determined by the state of the SCK pin (V_{IH} or V_{IL}) when the $\overline{CS}$ pin transitions from inactive (V_{IH}) to active (V_{IL}).

The HVC pin is high-voltage tolerant. To enter a high voltage command, the HVC pin must be greater than the V_{IHH} voltage.

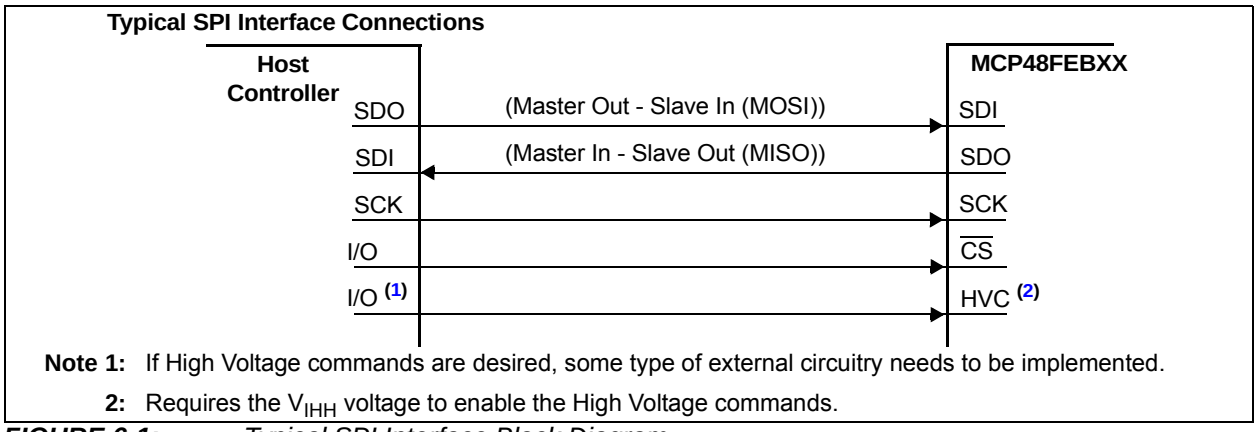
6.3 Communication Data Rates

The MCP48FEBXX supports clock rates (bit rate) of up to 20 MHz for write commands and 10 MHz for read commands.

For most applications, the write time will be considered more important, since that is how the device operation is controlled.

6.4 POR/BOR

On a POR/BOR event, the SPI Serial Interface Module state machine is reset, which includes that the Device's Memory Address pointer is forced to 00h.



Note 1: If High Voltage commands are desired, some type of external circuitry needs to be implemented.

2: Requires the V_{IHH} voltage to enable the High Voltage commands.

FIGURE 6-1: *Typical SPI Interface Block Diagram.*

6.5 Interface Pins (CS, SCK, SDI, SDO, and LAT/HVC)

The operation of the five interface pins and the High Voltage command (HVC) pin are discussed in this section. These pins are:

- SDI (Serial Data In)
- SDO (Serial Data Out)
- SCK (Serial Clock)
- CS (Chip Select)
- LAT/HVC (`High Voltage` command)

The serial interface works on either 8-bit or 24-bit boundaries depending on the selected command. The Chip Select (CS) pin frames the SPI commands.

6.5.1 SERIAL DATA IN (SDI)

The Serial Data In (SDI) signal is the data signal into the device. The value on this pin is latched on the rising edge of the SCK signal.

6.5.1.1 Serial Data Out (SDO)

The Serial Data Out (SDO) signal is the data signal out of the device. The value on this pin is driven on the falling edge of the SCK signal.

Once the CS pin is forced to the active level (V_{IL} or V_{IHH}), the SDO pin will be driven. The state of the SDO pin is determined by the serial bit's position in the command, the command selected, and if there is a command error state (CMDERR).

6.5.1.2 Serial Clock (SCK) (SPI Frequency Of Operation)

The SPI interface is specified to operate up to 20 MHz. The actual clock rate depends on the configuration of the system and the serial command used. Table 6-1 shows the SCK frequency for different configurations.

TABLE 6-1: SCK FREQUENCY

Memory Type Access		Command	
		Read	Write, Enable, Disable
Nonvolatile Memory	SDI, SDO	10 MHz	20 MHz (1, 2)
Volatile Memory	SDI, SDO	10 MHz	20 MHz (2)

Note 1: After a write command, the internal write cycle must complete before the next SPI command is received.
2: This is a design goal. The SDO pin performance is believed to be the limiting factor.

6.5.1.3 The CS Signal

The Chip Select (CS) signal is used to select the device and frame a command sequence. To start a command, or sequence of commands, the CS signal must transition from the inactive state (V_{IH}) to an active state (V_{IL} or V_{IHH}).

After the CS signal has gone active, the SDO pin is driven and the clock bit counter is reset.

Note: There is a required delay after the CS pin goes active to the 1st edge of the SCK pin.

If an error condition occurs for an SPI command, then the Command byte's Command Error (CMDERR) bit (on the SDO pin) will be driven low (V_{IL}). To exit the error condition, the user must take the CS pin to the V_{IH} level.

When the CS pin returns to the inactive state (V_{IH}), the SPI module resets (including the address pointer). While the CS pin is in the inactive state (V_{IH}), the serial interface is ignored. This allows the Host Controller to interface to other SPI devices using the same SDI, SDO, and SCK signals.

6.5.1.4 The HVC Signal

The high-voltage capability of the HVC pin allows High Voltage commands. High Voltage commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

6.5.2 THE SPI MODES

The SPI module supports two (of the four) standard SPI modes. These are Mode `0,0` and `1,1`. The mode is determined by the state of the SDI pin on the rising edge of the 1st clock bit (of the 8-bit byte).

6.5.2.1 Mode 0,0

In **Mode 0,0**:

- SCK idle state = low (V_{IL})
- Data is clocked in on the SDI pin on the rising edge of SCK
- Data is clocked out on the SDO pin on the falling edge of SCK

6.5.2.2 Mode 1,1

In **Mode 1,1**:

- SCK idle state = high (V_{IH})
- Data is clocked in on the SDI pin on the rising edge of SCK
- Data is clocked out on the SDO pin on the falling edge of SCK

7.0 SPI COMMANDS

This section documents the commands that the device supports.

The MCP48FEBXX's SPI command format supports 32 memory address locations and four commands. Commands may have two modes. These are:

- Normal Serial Commands
- High-Voltage Serial Commands

The four commands are:

- `Write` command (C1:C0 = '00')
- `Read` command (C1:C0 = '11')
- Commands to Modify the Device Configuration Bits:
  (HVC = V_{IHH})
  - `Enable Configuration Bit` (C1:C0 = '10')
  - `Disable Configuration Bit` (C1:C0 = '01')

The supported commands are shown in Table 7-1. These commands allow for both single data or continuous data operation. Table 7-1 also shows the required number of bit clocks for each command's different mode of operation.

Normal Serial commands are those where the HVC pin is driven to either V_{IH} or V_{IL}. With High-Voltage Serial commands, the HVC pin is driven to V_{IHH}.

The 8-bit commands (see Figure 7-1) are used to modify the device Configuration bits (**Enable Configuration Bit** and **Disable Configuration Bit**), while the 24-bit commands (see Figure 7-2) are used to read and write to the device registers (**Read Command** and **Write Command**). These commands contain a Command Byte and two Data Bytes.

Table 7-2 shows an overview of all the SPI commands and their interaction with other device features.

TABLE 7-1: SPI COMMANDS - NUMBER OF CLOCKS

Command					# of Bit Clocks (2)	Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second)			Comments
Operation	Code C1	Code C0	HV	Mode(1)		@ 1 MHz	@ 10 MHz	@ 20 MHz(3)	
Write Command	0	0	No(3)	Single	24	41,666	416,666	833,333	
	0	0	No(3)	Continuous	24 * n	41,666	416,666	833,333	For 10 data words
Read Command (4)	1	1	No(3)	Single	24	41,666	416,666	833,333	
	1	1	No(3)	Continuous	24 * n	41,666	416,666	833,333	For 10 data words
Enable Configuration Bit Command	1	0	Yes	Single	8	125,000	1,250,000	2,500,000	
	1	0	Yes	Continuous	8 * n	125,000	1,250,000	2,500,000	For 10 data words
Disable Configuration Bit Command	0	1	Yes	Single	8	125,000	1,250,000	2,500,000	
	0	1	Yes	Continuous	8 * n	125,000	1,250,000	2,500,000	For 10 data words

Note 1: Nonvolatile registers can only use the "Single" mode.

2: "n" indicates the number of times the command operation is to be repeated.

3: If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

4: This command is useful to determine when an EEPROM programming cycle has completed.

7.0.1 COMMAND BYTE

The command byte has three fields: the address, the command, and one data bit (see Figure 7-1). Currently only one of the data bits is defined (D8). This is for the `Write` command.

The device memory is accessed when the master sends a proper command byte to select the desired operation. The memory location getting accessed is contained in the command byte's AD4:AD0 bits. The action desired is contained in the command byte's C1:C0 bits, see Table 7-2. C1:C0 determines if the desired memory location will be read, written, enabled or disabled.

As the command byte is being loaded into the device (on the SDI pin), the device's SDO pin is driving. The SDO pin will output high bits for the first seven bits of that command. On the 8th bit, the SDO pin will output the CMDERR bit state (see **Section 7.0.3 "Error Condition"**).

7.0.2 DATA BYTES

Data bytes are only present in the `Read` and the `Write` commands. These commands concatenate the two data bytes after the command byte, for a 24-bit long command (see Figure 7-1).

TABLE 7-2: COMMAND BIT OVERVIEW

C1:C0 Bit States	Command	# of Bits	Normal or HV
11	Read Data	24-Bits	Normal
00	Write Data	24-Bits	Normal
01	Enable (1)	8-Bits	HV Only
10	Disable (1)	8-Bits	HV Only

Note 1: High Voltage enable and disable commands on select nonvolatile memory locations.

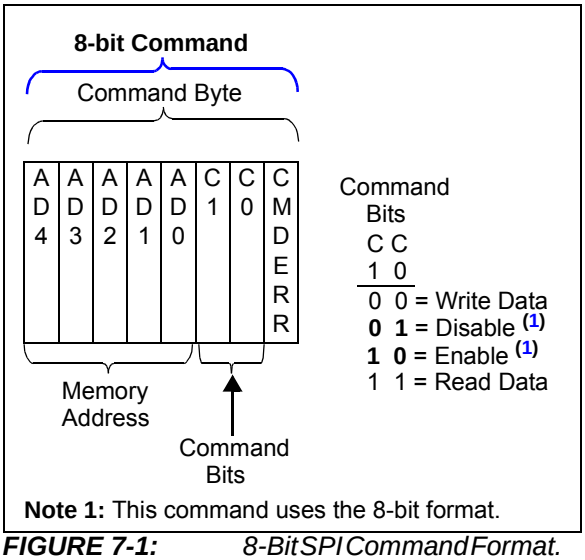


FIGURE 7-1: *8-Bit SPI Command Format.*

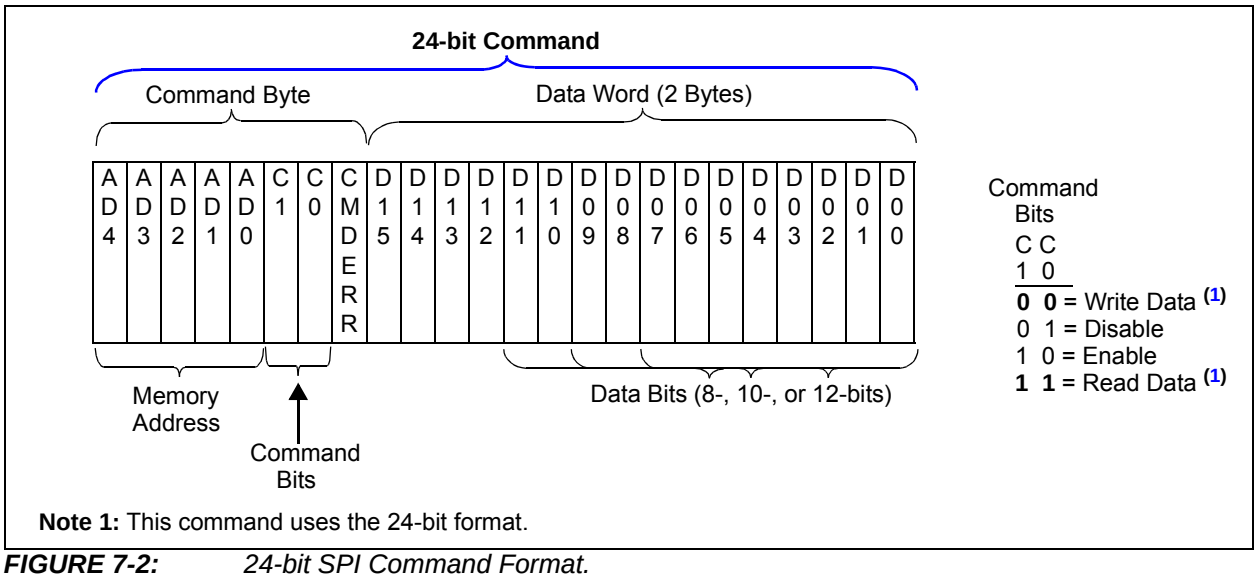


FIGURE 7-2: *24-bit SPI Command Format.*

7.0.3 ERROR CONDITION

The Command Error (CMDERR) bit indicates if the five address bits received (AD4:AD0) and the two command bits received (C1:C0) are a valid combination (see Figures 7-1 and 7-2). The CMDERR bit is high if the combination is valid and low if the combination is invalid.

The Command Error bit will also be low if a write to a nonvolatile address has been specified and another SPI command occurs before the $\overline{CS}$ pin is driven inactive (V_{IH}).

SPI commands that do not have a multiple of eight clocks are ignored.

Once an error condition has occurred, any following commands are ignored. All following SDO bits will be low until the CMDERR condition is cleared by forcing the $\overline{CS}$ pin to the inactive state (V_{IH}).

7.0.3.1 Aborting a Transmission

All SPI transmissions must have the correct number of SCK pulses to be executed. The command is not executed until the complete number of clocks have been received. Some commands also require the $\overline{CS}$ pin to be forced inactive (V_{IH}). If the $\overline{CS}$ pin is forced to the inactive state (V_{IH}), the serial interface is reset. Partial commands are not executed.

SPI is more susceptible to noise than other bus protocols. The most likely case is that noise corrupts the value of the data being clocked into the MCP48FEBXX or the SCK pin is injected with extra clock pulses. This may cause data to be corrupted in the device, or a Command Error to occur, since the address and command bits were not a valid combination. The extra SCK pulse will also cause the SPI data ($\overline{SDI}$) and clock (SCK) to be out of sync. Forcing the $\overline{CS}$ pin to the inactive state (V_{IH}) resets the serial interface. The SPI interface will ignore activity on the SDI and SCK pins until the $\overline{CS}$ pin transition to the active state is detected (V_{IH} to V_{IL} or V_{IH} to V_{IHH}).

Note 1: When data is not being received by the MCP48FEBXX, it is recommended that the $\overline{CS}$ pin be forced to the inactive level (V_{IL}).

2: It is also recommended that long continuous command strings be broken down into single commands or shorter continuous command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI commands.

7.0.4 CONTINUOUS COMMANDS

The device supports the ability to execute commands continuously. While the $\overline{CS}$ pin is in the active state (V_{IL}), any sequence of valid commands may be received.

The following example is a valid sequence of events:

1. $\overline{CS}$ pin driven active (V_{IL})
2. `Read` command
3. `Write` command (Volatile memory)
4. `Write` command (Nonvolatile memory)
5. $\overline{CS}$ pin driven inactive (V_{IH})

Note 1: It is recommended that while the $\overline{CS}$ pin is active, only one type of command should be issued. When changing commands, it is advisable to take the $\overline{CS}$ pin inactive then force it back to the active state.

2: It is also recommended that long command strings should be broken down into shorter command strings. This reduces the probability of noise on the SCK pin, corrupting the desired SPI command string.

7.1 Write Command

Write commands are used to transfer data to the desired memory location (from the Host controller). The `Write` command can be issued to both the volatile and nonvolatile memory locations.

Write commands can be structured as either Single or Continuous.

The format of the command is shown in Figures 7-3 (Single) and 7-4 (Continuous).

A write command to a volatile memory location changes that location after a properly formatted write command has been received.

A write command to a nonvolatile memory location will start an EEPROM write cycle only after a properly formatted write command has been received and the $\overline{CS}$ pin transitions to the inactive state (V_{IH}).

Note 1:	Writes to certain memory locations will be dependent on the state of the WiperLock™ technology status bits.
2:	During device communication, if the Device Address/Command combination is invalid or an unimplemented Device Address is specified, then the MCP48FEBXX will generate a Command Error state. To reset the SPI state machine, the $\overline{CS}$ pin must transition to the inactive state (V_{IH}).

7.1.1 SINGLE WRITE TO VOLATILE MEMORY

The write operation requires that the $\overline{CS}$ pin be in the active state (V_{IL}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL}). The 24-bit `Write` command (Command Byte and Data Bytes) is then clocked in on the SCK and SDI pins. Once all 24 bits have been received, the specified volatile address is updated. A write will not occur if the `Write` command isn't exactly 24 clock pulses. This protects against system issues corrupting the nonvolatile memory locations.

Figures 7-5 and 7-6 show the waveforms for a single write (depending on SPI mode).

7.1.2 SINGLE WRITE TO NONVOLATILE MEMORY

The sequence to write to a single nonvolatile memory location is the same as a single write to volatile memory with the exception that after the $\overline{CS}$ pin is driven inactive (V_{IH}), the EEPROM write cycle (t_{WC}) is started. A write cycle will not start if the `Write` command isn't exactly 24 clock pulses. This protects against system issues corrupting the nonvolatile memory locations.

Once a write command to a nonvolatile memory location has been received, no other SPI commands should be received before the $\overline{CS}$ pin transitions to the inactive state (V_{IH}), or the current SPI command will have a Command Error (CMDERR) occur.

After the $\overline{CS}$ pin is driven inactive (V_{IH}), the serial interface may immediately be re-enabled by driving the $\overline{CS}$ pin to the active state (V_{IL}).

During an EEPROM write cycle, access to the volatile memory is allowed when using the appropriate command sequence. Commands that address nonvolatile memory are ignored until the EEPROM write cycle (t_{WC}) completes. This allows the Host Controller to operate on the volatile DAC registers.

Note:	The EEWA status bit indicates if an EEPROM write cycle is active (see Register 4-4).

Figures 7-5 and 7-6 show the waveforms for a single write (depending on the SPI mode).

7.1.3 CONTINUOUS WRITES TO VOLATILE MEMORY

A Continuous Write mode of operation is possible when writing to the device's volatile memory registers (see Table 7-3). Figure 7-4 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

TABLE 7-3: VOLATILE MEMORY ADDRESSES

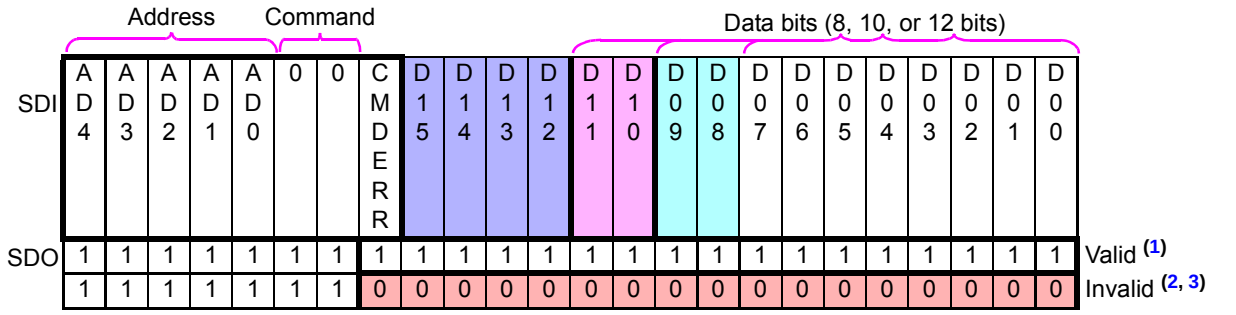
Address	Single-Channel	Dual-Channel
00h	Yes	Yes
01h	**No**	Yes
08h	Yes	Yes
09h	Yes	Yes
0Ah	Yes	Yes

7.1.4 CONTINUOUS WRITES TO NONVOLATILE MEMORY

Continuous writes to nonvolatile memory are not allowed, and attempts to do so will result in a Command Error (CMDERR) condition.

7.1.5 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

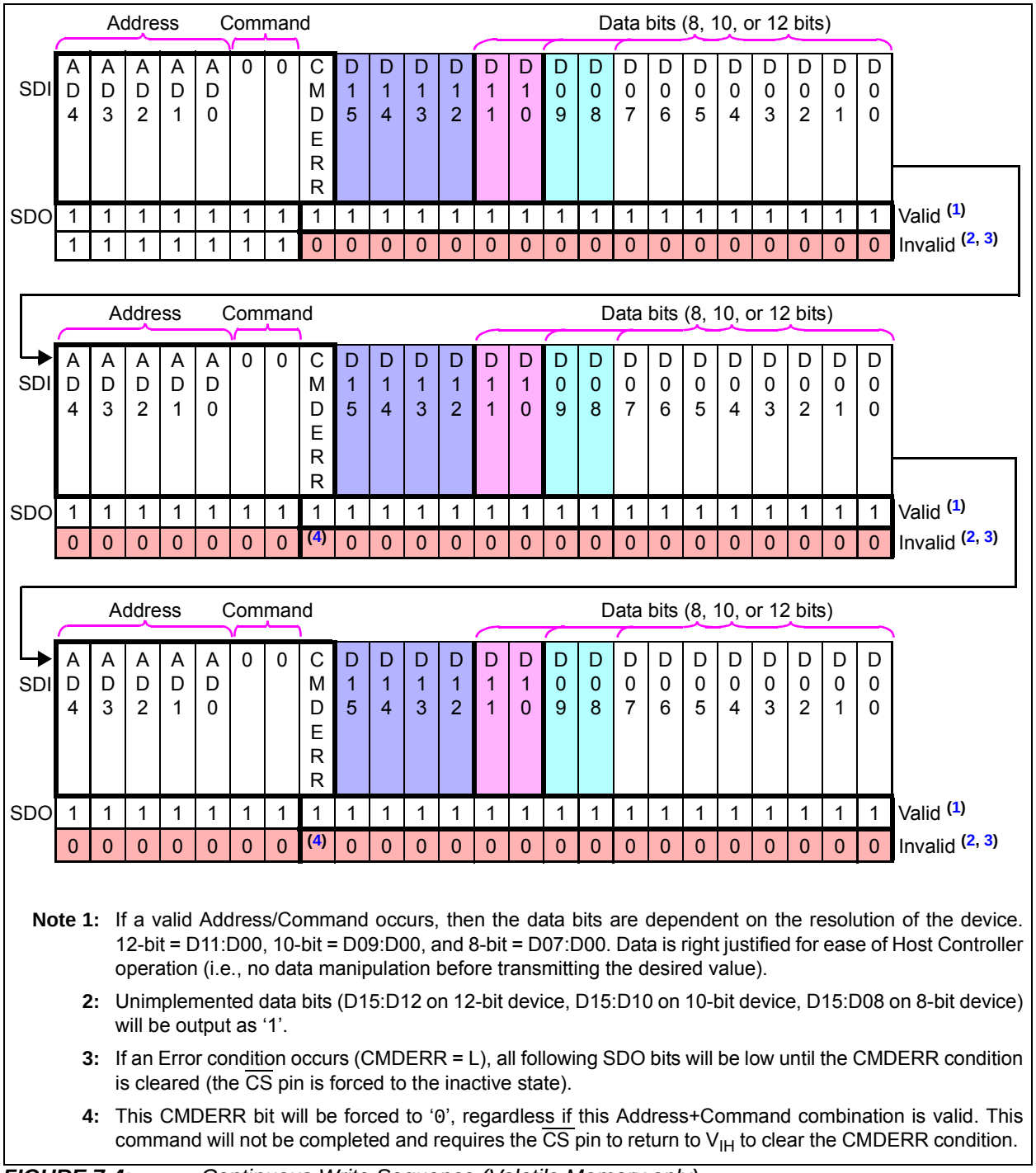


Note 1: If a valid Address/Command occurs, then the data bits are dependent on the resolution of the device. 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. Data is right justified for ease of Host Controller operation (i.e., no data manipulation before transmitting the desired value).

2: Unimplemented data bits (D15:D12 on 12-bit device, D15:D10 on 10-bit device, D15:D08 on 8-bit device) will be output as '1'.

3: If an Error condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

FIGURE 7-3: *Write Command - SDI and SDO States.*



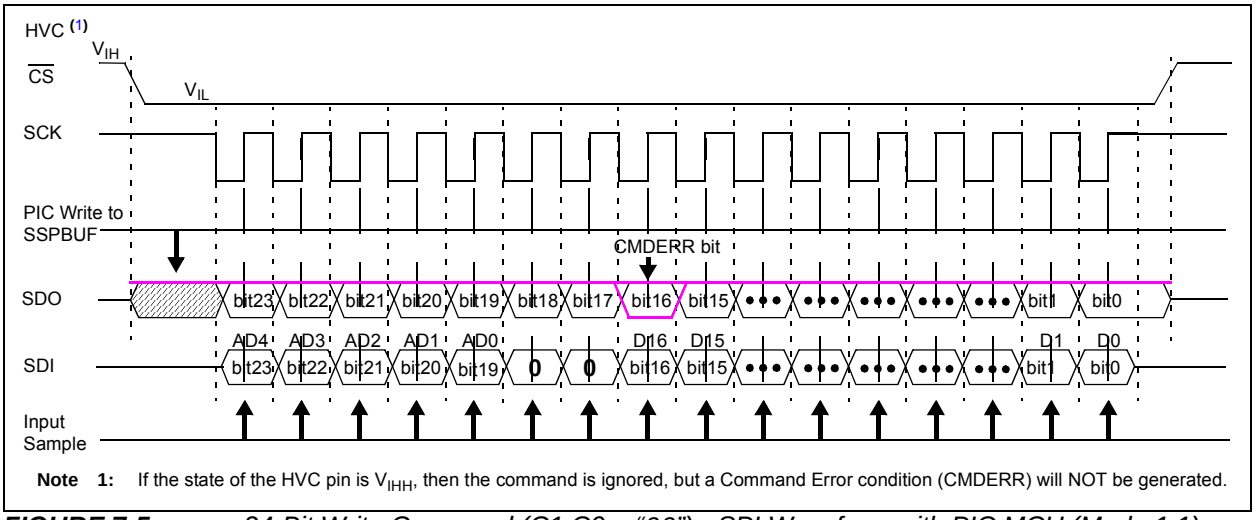
Note 1: If a valid Address/Command occurs, then the data bits are dependent on the resolution of the device. 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. Data is right justified for ease of Host Controller operation (i.e., no data manipulation before transmitting the desired value).

2: Unimplemented data bits (D15:D12 on 12-bit device, D15:D10 on 10-bit device, D15:D08 on 8-bit device) will be output as '1'.

3: If an Error condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

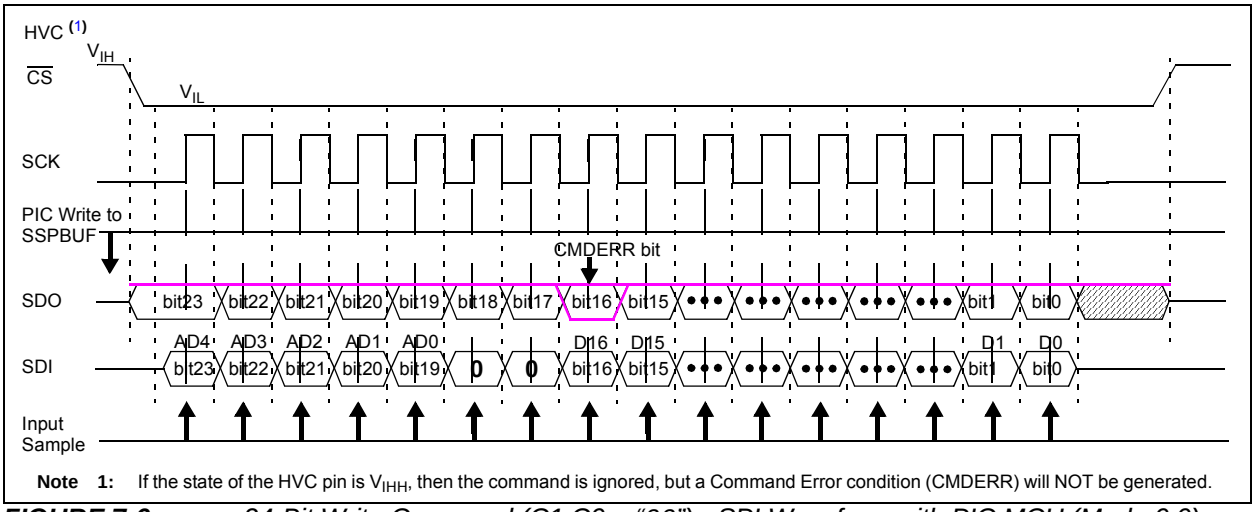
4: This CMDERR bit will be forced to '0', regardless if this Address+Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-4: *Continuous Write Sequence (Volatile Memory only).*



Note 1: If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

FIGURE 7-5: *24-Bit Write Command (C1:C0 = "00") - SPI Waveform with PIC MCU (Mode 1,1).*



Note 1: If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

FIGURE 7-6: *24-Bit Write Command (C1:C0 = "00") - SPI Waveform with PIC MCU (Mode 0,0).*

7.2 Read Command

The Read command is a 24-bit command and is used to transfer data from the specified memory location to the Host controller. The Read command can be issued to both the volatile and nonvolatile memory locations. The format of the command as well as an example SDI and SDO data is shown in Figure 7-7.

The first 7-bits of the Read command determine the address and the command. The 8th clock will output the CMDERR bit on the SDO pin. By means of the remaining 16 clocks, the device will transmit the data bits of the specified address (AD4:AD0).

During an EEPROM write cycle (write to nonvolatile memory location or Enable/Disable Configuration Bit command), the Read command can only read the volatile memory locations. By reading the Status Register (0Ah), the Host Controller can determine when the write cycle has completed (via the state of the EEWA bit)

The Read command formats include:

- **Single Read**
- **Continuous Reads**

Note 1: During device communication, if the Device Address/Command combination is invalid or an unimplemented Address is specified, then the MCP48FEBXX will command error that byte. To reset the SPI state machine, the $\overline{CS}$ pin must be driven to the V_{IH} state.

2: If the LAT pin is High (V_{IH}), reads of the volatile DAC Register read the output value, not the internal register.

3: The read commands operate the same regardless of the state of the High-Voltage Command (HVC) signal.

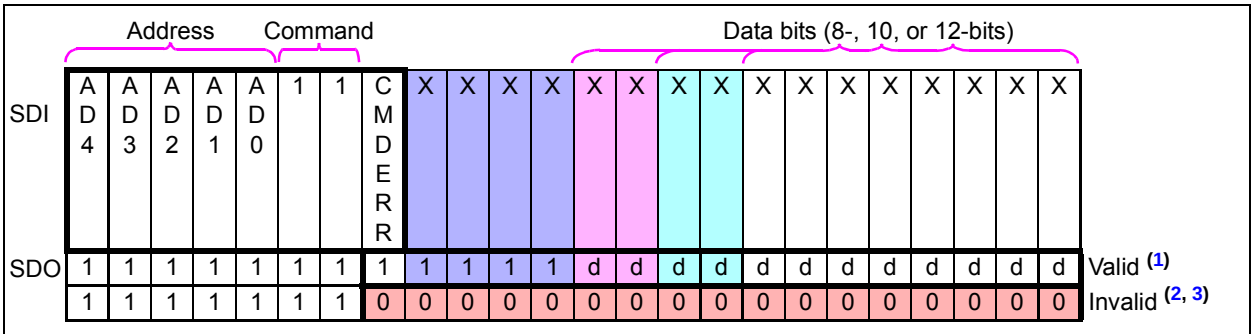
7.2.1 LAT PIN INTERACTION

During a Read command of the DACx Registers, if the LAT pin transitions from V_{IH} to V_{IL}, then the read data may be corrupted. This is due to the fact that the data being read is the output value and not the DAC register value. The LAT pin transition causes an update of the output value. Based on the DAC output value, the DACx register value, and the Command bit where the LAT pin transitions, the value being read could be corrupted.

If LAT pin transitions occur during a read of the DACx register, it is recommended that sequential reads be performed until the two most recent read values match. Then the most recent read data is good.

7.2.2 SINGLE READ

The Read command operation requires that the $\overline{CS}$ pin be in the active state (V_{IL}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL}). The 24-bit Read command (Command Byte and Data Byte) is then clocked in on the SCK and SDI pins. The SDO pin starts driving data on the 8th bit (CMDERR bit), and the addressed data comes out on the 9th through 24th clocks.



Note 1: If a valid Address/Command occurs, then the data bits are dependent on the resolution of the device. 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. Data is right justified for ease of Host Controller operation (i.e., no data manipulation before transmitting the desired value).

2: Unimplemented data bits (D15:D12 on 12-bit device, D15:D10 on 10-bit device, D15:D08 on 8-bit device) will be output as '1'.

3: If an Error condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

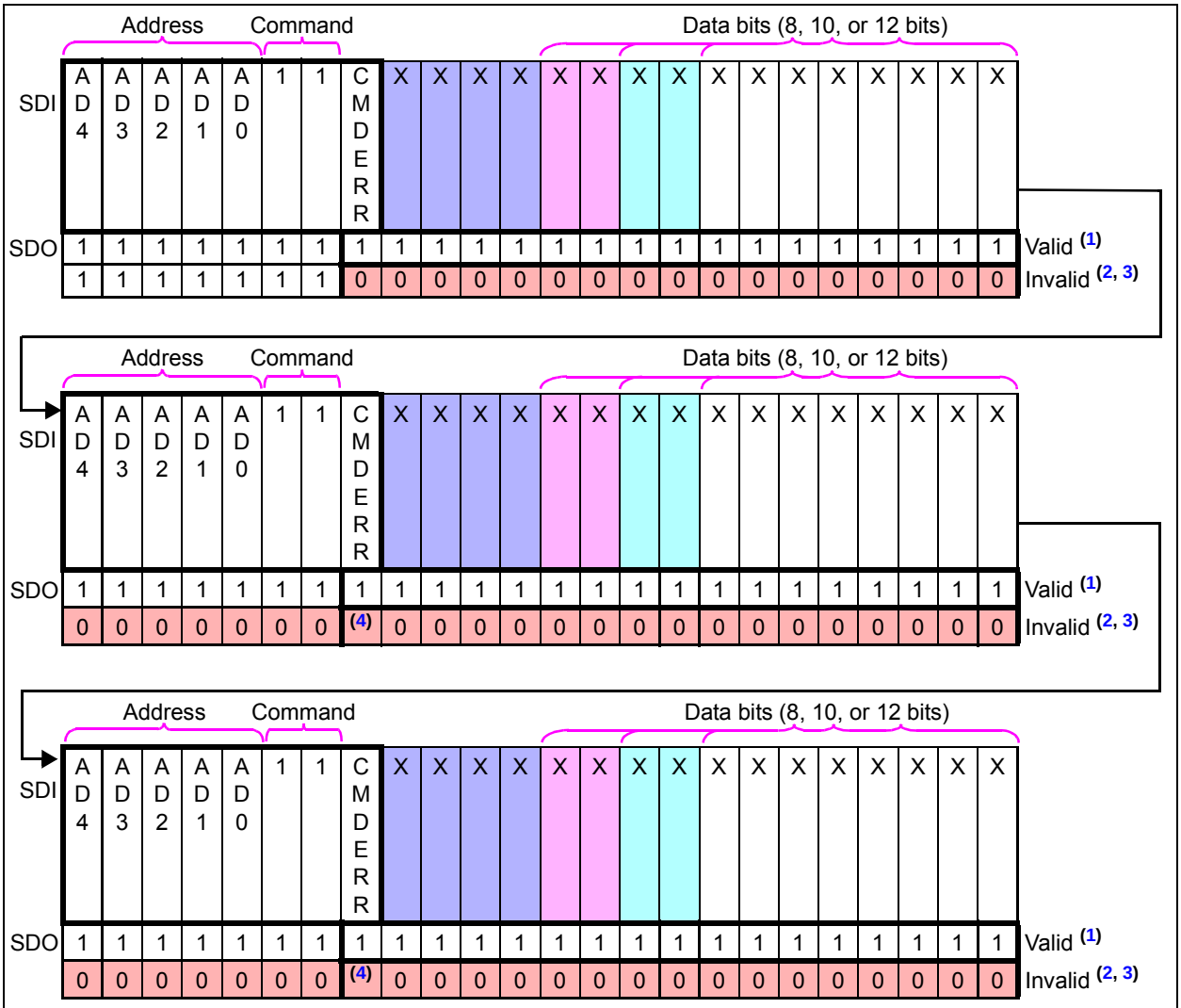
FIGURE 7-7: *Read Command - SDI and SDO States.*

7.2.3 CONTINUOUS READS

Continuous-reads format allows the device's memory to be read quickly. Continuous reads are possible to all memory locations. If a nonvolatile memory write cycle is occurring, then read commands may only access the volatile memory locations.

Figure 7-8 shows the sequence for three continuous reads. The reads do not need to be to the same memory address.

This is useful in reading the System Status register (0Ah) to determine if an EEPROM write cycle has completed (EEWA bit).



Note 1: If a valid Address/Command occurs, then the data bits are dependent on the resolution of the device. 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. Data is right justified for ease of Host Controller operation (i.e., no data manipulation before transmitting the desired value).

2: Unimplemented data bits (D15:D12 on 12-bit device, D15:D10 on 10-bit device, D15:D08 on 8-bit device) will be output as '1'.

3: If an Error condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

4: This CMDERR bit will be forced to '0', regardless if this Address+Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-8: *Continuous-Reads Sequence.*

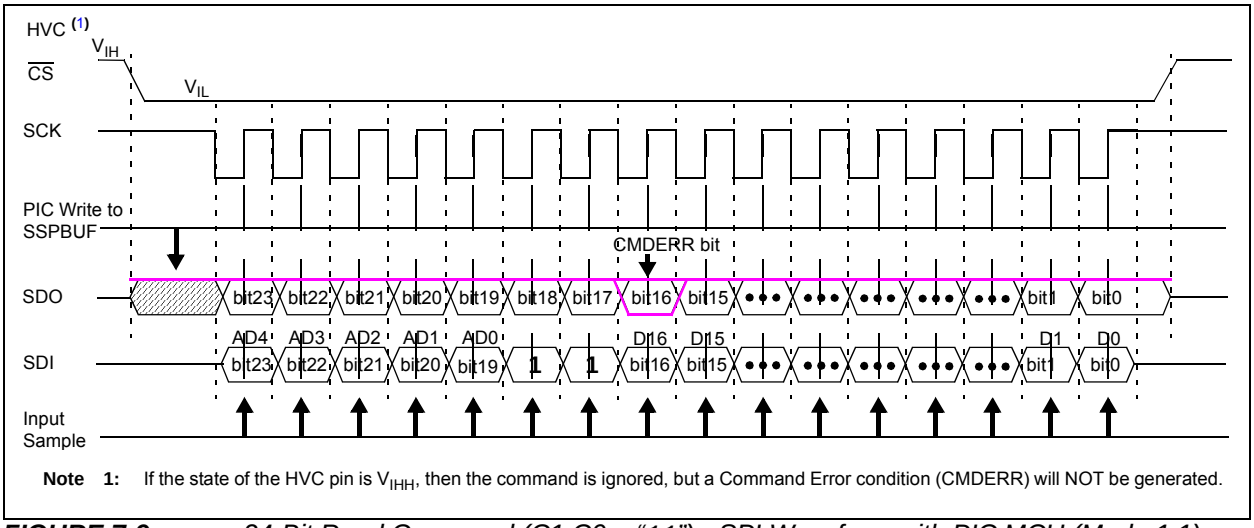


FIGURE 7-9: *24-Bit Read Command (C1:C0 = "11") - SPI Waveform with PIC MCU (Mode 1,1).*

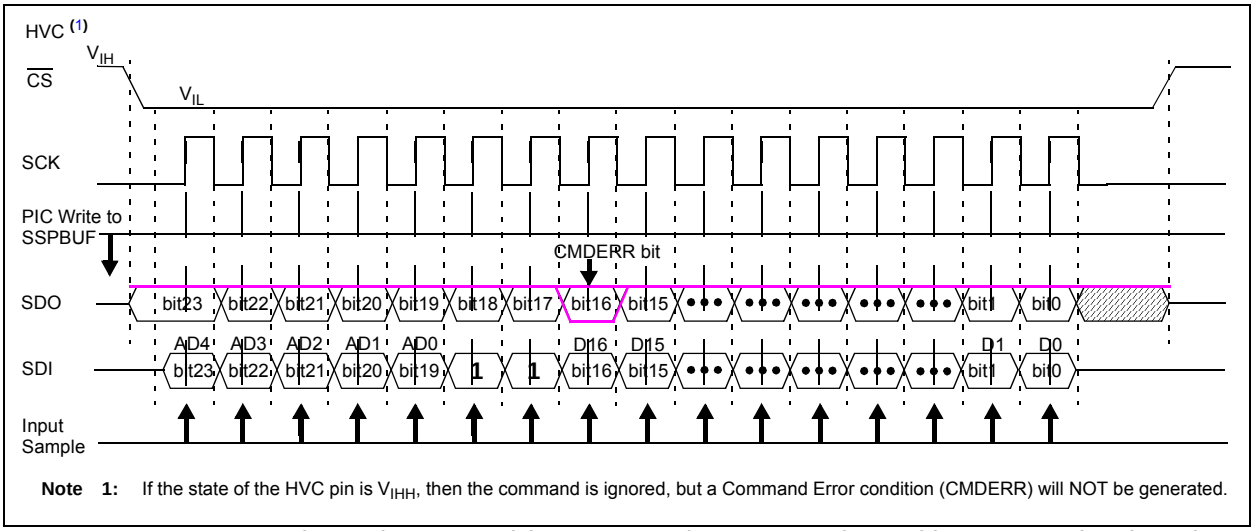


FIGURE 7-10: *24-Bit Read Command (C1:C0 = "11") - SPI Waveform with PIC MCU (Mode 0,0).*

7.3 Commands to Modify the Device Configuration Bits

The MCP48FEBXX devices support two commands which are used to program the device's configuration bits. These commands require a high voltage (V_{IHH}) on the HVC pin. These commands are:

- **Enable Configuration Bit**
- **Disable Configuration Bit**

The configuration bits are used to inhibit the DAC values from inadvertent modification. High voltage is required to change the state of these bits if/when the DAC values need to be modified.

7.4 Enable Configuration Bit (High Voltage)

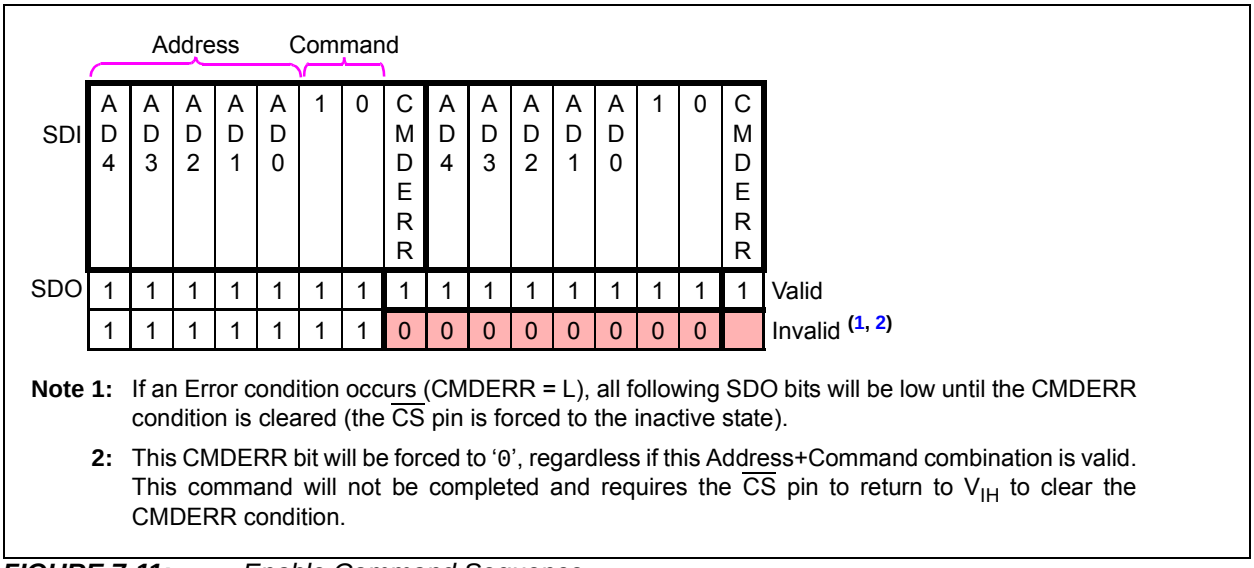
Figure 7-11 (Enable) shows the formats for a single `Enable Configuration Bit` command. The command will only start the EEPROM write cycle (t_{WC}) after a properly formatted command has been received.

During an EEPROM write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes. This allows the Host Controller to operate on the volatile DAC, the volatile V_{REF}, Power-Down, Gain and Status, and WiperLock Technology Status registers. The EEWA bit in the Status register indicates the status of the EEPROM write cycle.

7.4.1 HIGH-VOLTAGE COMMAND (HVC) SIGNAL

The High-Voltage Command (HVC) signal is used to indicate that the command, or sequence of commands, are in the High-Voltage mode. Signals higher than V_{IHH} (~9.0V) on the $\overline{LAT}$/HVC pin puts the device into High-Voltage mode. High-Voltage commands allow the device's WiperLock technology and write-protect features to be enabled and disabled.

Note 1: There is a required delay after the HVC pin is driven to the V_{IHH} level on the 1st edge of the SCK pin.



Note 1: If an Error condition occurs ($\overline{CMDERR}$ = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

2: This CMDERR bit will be forced to '0', regardless if this Address+Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-11: *Enable Command Sequence.*

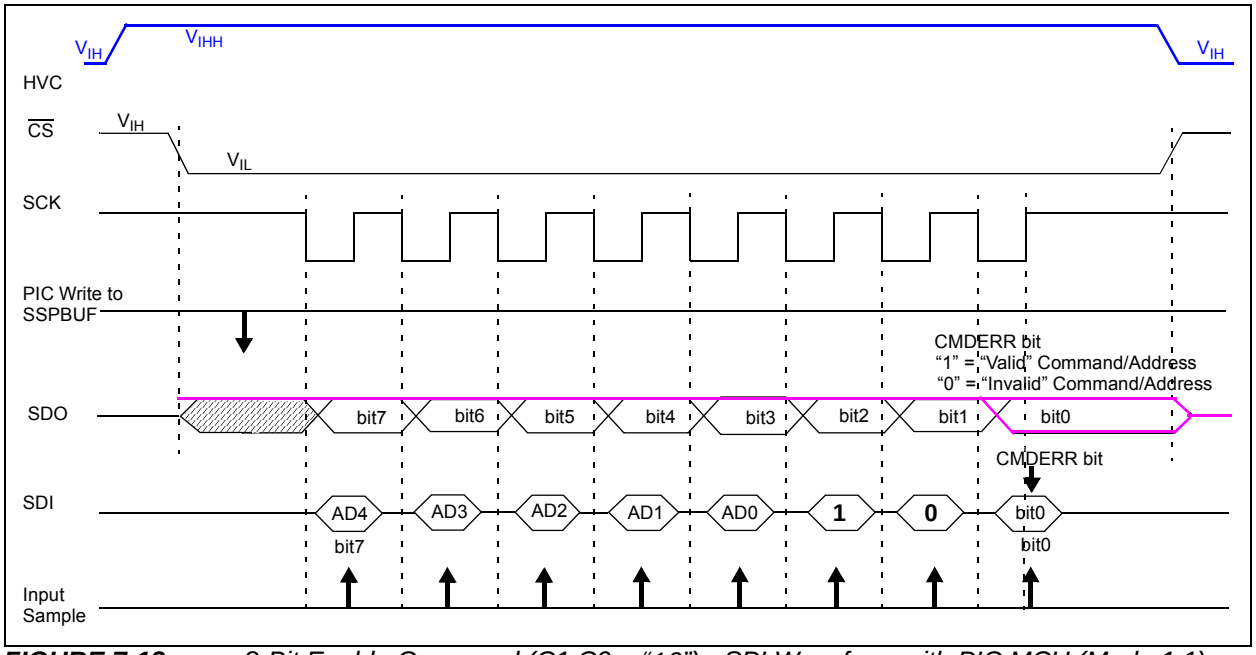


FIGURE 7-12: *8-Bit Enable Command (C1:C0 = "10") - SPI Waveform with PIC MCU (Mode 1,1).*

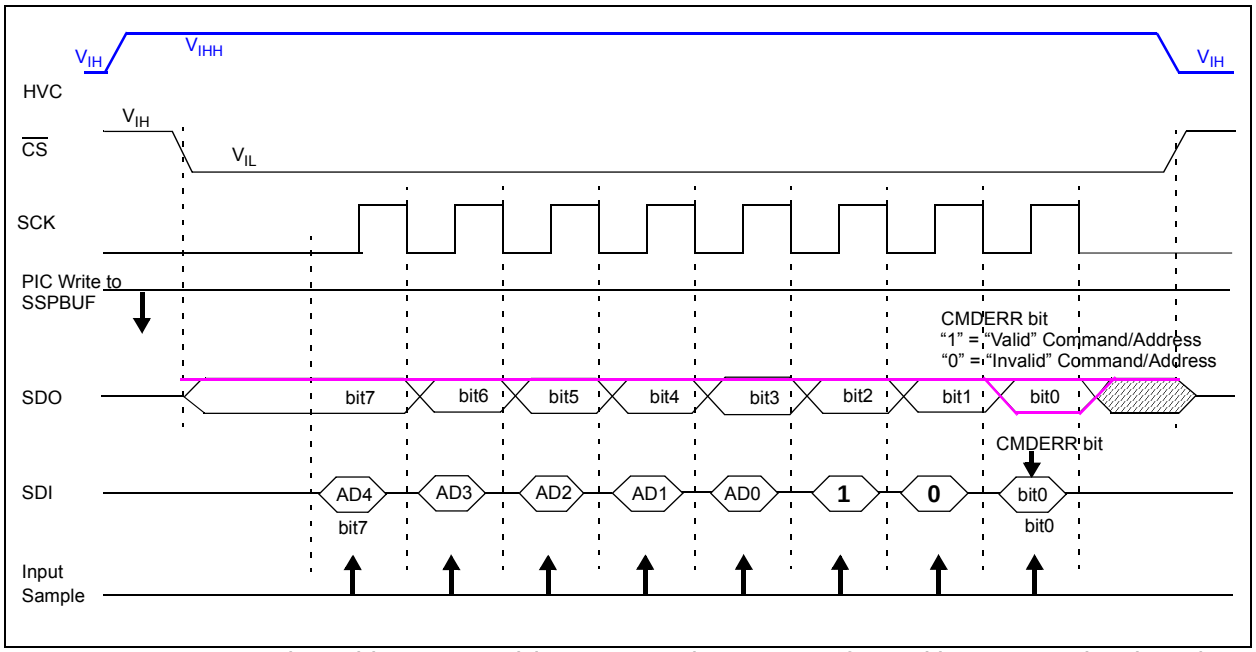


FIGURE 7-13: *8-Bit Enable Command (C1:C0 = "10") - SPI Waveform with PIC MCU (Mode 0,0).*

7.5 Disable Configuration Bit (High Voltage)

Figure 7-14 (Disable) shows the formats for a single `Disable Configuration Bit` command. The command will only start an EEPROM write cycle (t_{WC}) after a properly formatted command has been received.

During an EEPROM write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes. This allows the Host Controller to operate on the volatile DAC, the volatile V_{REF}, Power-Down, Gain and Status, and WiperLock Technology Status registers. The EEWA bit in the Status register indicates the status of an EEPROM write cycle.

7.5.1 HIGH-VOLTAGE COMMAND (HVC) SIGNAL

The High-Voltage Command (HVC) signal is used to indicate that the command, or sequence of commands, are in the High-Voltage mode. Signals higher than V_{IHH} (~9.0V) on the HVC pin puts the MCP48FEBXX devices into High-Voltage mode. High Voltage commands allow the device's WiperLock technology and write protect features to be enabled and disabled.

Note 1: There is a required delay after the HVC pin is driven to the V_{IHH} level to the 1st edge of the SCK pin.

	Address					Command											
SDI	AD4	AD3	AD2	AD1	AD0	0	1	CMDERR	AD4	AD3	AD2	AD1	AD0	0	1	CMDERR	
SDO	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Valid
	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0		Invalid (1, 2)

Note 1: If an Error condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

2: This CMDERR bit will be forced to '0', regardless if this Address+Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-14: *Disable Command Sequence.*

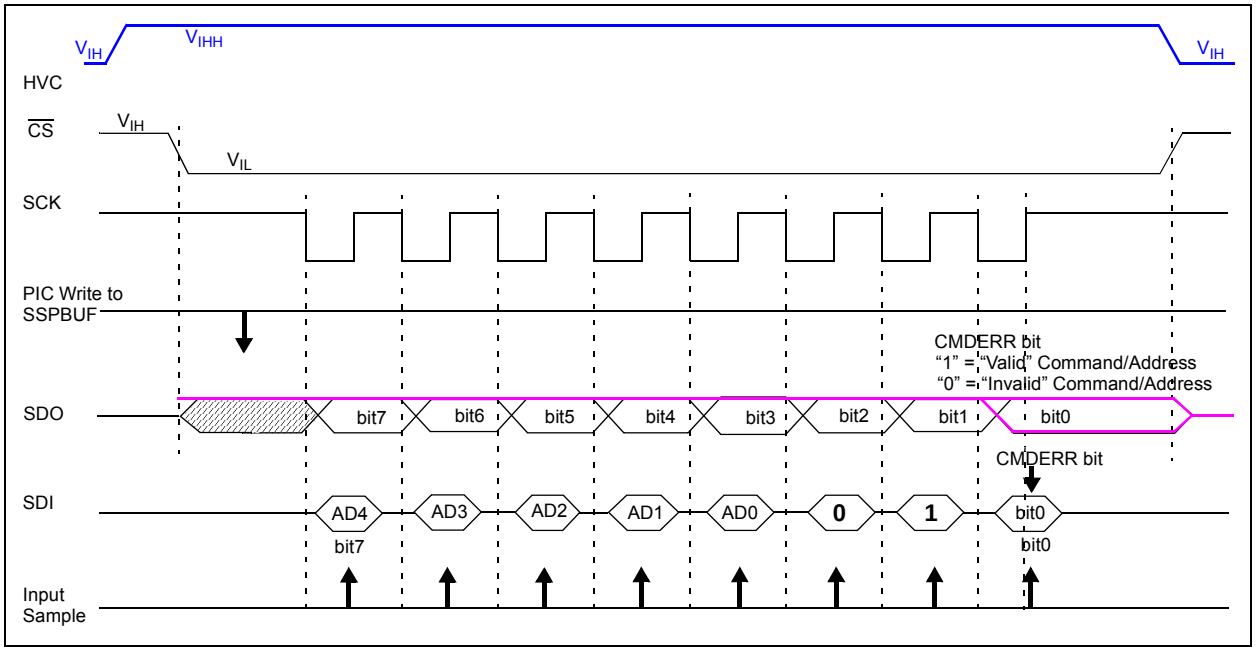


FIGURE 7-15: *8-Bit Disable Command (C1:C0 = "01") - SPI Waveform with PIC MCU (Mode 1,1).*

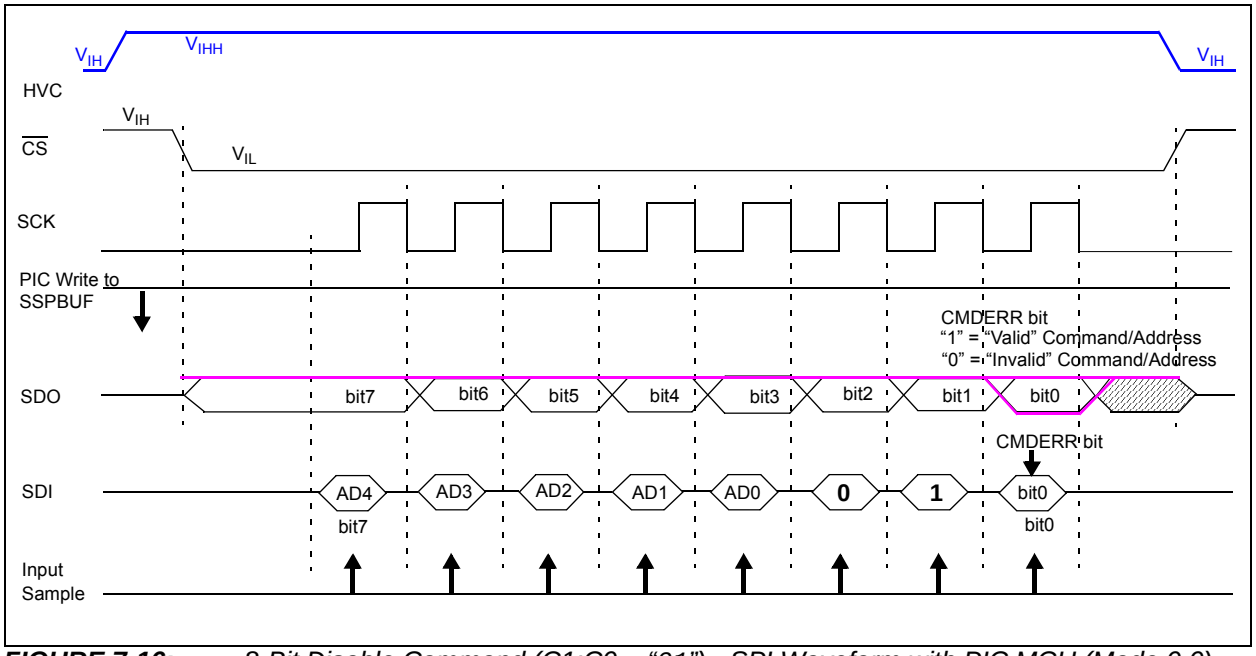


FIGURE 7-16: *8-Bit Disable Command (C1:C0 = "01") - SPI Waveform with PIC MCU (Mode 0,0).*

8.0 TYPICAL APPLICATIONS

The MCP48FEBXX family of devices are general purpose, single/dual-channel voltage output DACs for various applications where a precision operation with low power and nonvolatile EEPROM memory is needed.

Since the devices include a nonvolatile EEPROM memory, the user can utilize these devices for applications that require the output to return to the previous setup value on subsequent power-ups.

Applications generally suited for the devices are:

- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery-Powered)
- Motor Control

8.1 Power Supply Considerations

The power source should be as clean as possible. The power supply to the device is also used for the DAC voltage reference internally if the internal V_{DD} is selected as the resistor ladder's reference voltage (VRxB:VRxA = '00').

Any noise induced on the V_{DD} line can affect the DAC performance. Typical applications will require a bypass capacitor in order to filter out high-frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-1 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors should be placed as close to the V_{DD} pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the device should reside on the analog plane.

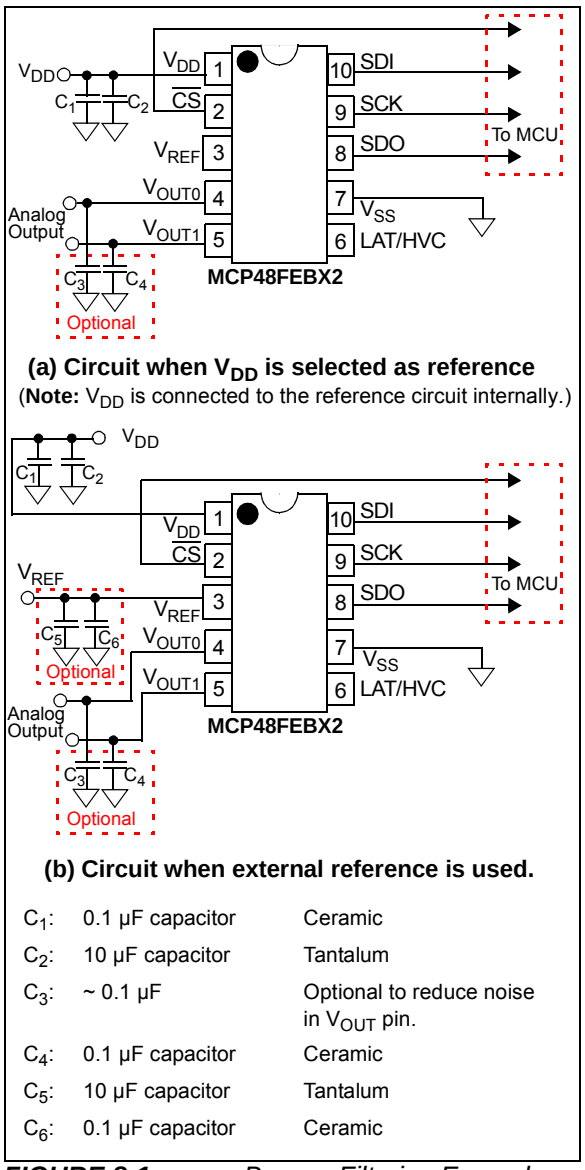


FIGURE 8-1: *Bypass Filtering Example Circuit.*

8.2 Application Examples

The MCP48FEBXX devices are rail-to-rail output DACs designed to operate with a V_{DD} range of 2.7V to 5.5V. The internal output operational amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of external buffers for most applications. The user can use gain of 1 or 2 of the output operational amplifier by setting the Configuration register bits. Also, the user can use internal V_{DD} as the reference or use an external reference. Various user options and easy-to-use features make the devices suitable for various modern DAC applications.

Application examples include:

- Decreasing Output Step Size
- Building a “Window” DAC
- Bipolar Operation
- Selectable Gain and Offset Bipolar Voltage Output
- Designing a Double-Precision DAC
- Building Programmable Current Source
- Serial Interface Communication Times
- Power Supply Considerations
- Layout Considerations

8.2.1 DC SET POINT OR CALIBRATION

A common application for the devices is a digitally-controlled set point and/or calibration of variable parameters, such as sensor offset or slope. For example, the MCP48FEB2X provides 4096 output steps. If voltage reference is 4.096V (where Gx = ‘0’), the LSb size is 1 mV. If a smaller output step size is desired, a lower external voltage reference is needed.

8.2.1.1 Decreasing Output Step Size

If the application is calibrating the bias voltage of a diode or transistor, a bias voltage range of 0.8V may be desired with about 200 µV resolution per step. Two common methods to achieve small step size are:

- **Using Lower V_{ref} Pin Voltage:** Using an external voltage reference (V_{REF}) is an option if the external reference is available with the desired output voltage range. However, occasionally, when using a low-voltage reference voltage, the noise floor causes a SNR error that is intolerable.
- **Using A Voltage Divider On The DAC’s Output:** Using a voltage divider provides some advantages when external voltage reference needs to be very low or when the desired output voltage is not available. In this case, a larger value reference voltage is used while two resistors scale the output range down to the precise desired level.

Figure 8-2 illustrates this concept. A bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

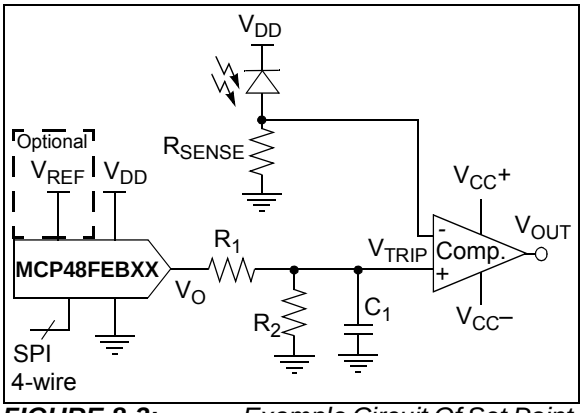


FIGURE 8-2: *Example Circuit Of Set Point or Threshold Calibration.*

EQUATION 8-1: V_{OUT} AND V_{TRIP} CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{trip} = V_{OUT}\left(\frac{R_2}{R_1 + R_2}\right)$$

8.2.1.2 Building a “Window” DAC

When calibrating a set point or threshold of a sensor, typically only a small portion of the DAC output range is utilized. If the LSb size is adequate enough to meet the application’s accuracy needs, the unused range is sacrificed without consequences. If greater accuracy is needed, then the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near V_{REF}, 2 • V_{REF}, or V_{SS}, then creating a “window” around the threshold has several advantages. One simple method to create this “window” is to use a voltage divider network with a pull-up and pull-down resistor. Figure 8-3 and Figure 8-5 illustrate this concept.

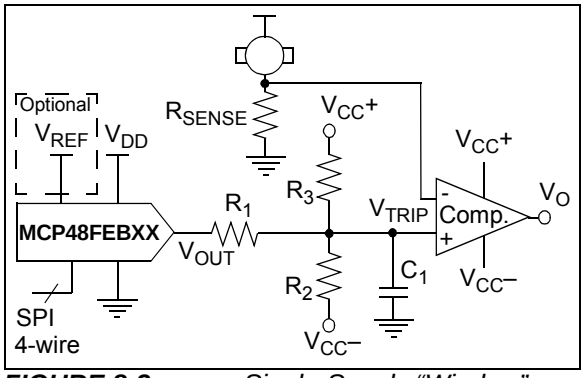


FIGURE 8-3: *Single-Supply “Window” DAC.*

EQUATION 8-2: V_{OUT} AND V_{TRIP} CALCULATIONS

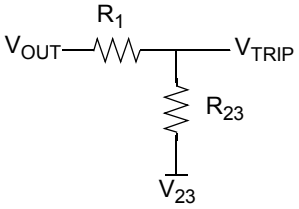
$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{TRIP} = \frac{V_{OUT}R_{23} + V_{23}R_1}{R_1 + R_{23}}$$

Thevenin Equivalent:

$$R_{23} = \frac{R_2R_3}{R_2 + R_3}$$

$$V_{23} = \frac{(V_{CC+}R_2) + (V_{CC-}R_3)}{R_2 + R_3}$$



8.3 Bipolar Operation

Bipolar operation is achievable by utilizing an external operational amplifier. This configuration is desirable due to the wide variety and availability of op amps. This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Figure 8-4 illustrates a simple bipolar voltage source configuration. R_1 and R_2 allow the gain to be selected, while R_3 and R_4 shift the DAC's output to a selected offset. Note that R4 can be tied to V_{DD} instead of V_{SS} if a higher offset is desired.

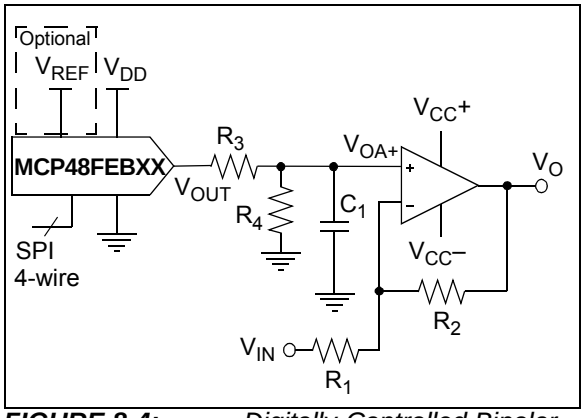


FIGURE 8-4: *Digitally-Controlled Bipolar Voltage Source Example Circuit.*

EQUATION 8-3: V_{OUT}, V_{OA+}, AND V_O CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4}{R_3 + R_4}$$

$$V_O = V_{OA+} \bullet (1 + \frac{R_2}{R_1}) - V_{DD} \bullet (\frac{R_2}{R_1})$$

8.4 Selectable Gain and Offset Bipolar Voltage Output

In some applications, precision digital control of the output range is desirable. Figure 8-5 illustrates how to use DAC devices to achieve this in a bipolar or single-supply application.

This circuit is typically used for linearizing a sensor whose slope and offset varies.

The equation to design a bipolar "window" DAC would be utilized if R_3, R_4 and R_5 are populated.

Bipolar DAC Example

An output step size of 1 mV with an output range of ±2.05V is desired for a particular application.

Step 1: Calculate the range: +2.05V – (-2.05V) = 4.1V.

Step 2: Calculate the resolution needed:

4.1V/1 mV = 4100

Since 2^{12} = 4096, 12-bit resolution is desired.

Step 3: The amplifier gain (R_2/R_1), multiplied by full-scale V_{OUT} (4.096V), must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values ($R_1 + R_2$), the V_{REF} value must be selected first. If a V_{REF} of 4.096V is used, solve for the amplifier's gain by setting the DAC to 0, knowing that the output needs to be -2.05V.

The equation can be simplified to:

EQUATION 8-4:

$$\frac{-R_2}{R_1} = \frac{-2.05}{4.096V} \qquad \frac{R_2}{R_1} = \frac{1}{2}$$

If R_1 = 20 kΩ and R_2 = 10 kΩ, the gain will be 0.5.

Step 4: Next, solve for R_3 and R_4 by setting the DAC to 4096, knowing that the output needs to be +2.05V.

EQUATION 8-5:

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot 4.096V)}{1.5 \cdot 4.096V} = \frac{2}{3}$$

If R_4 = 20 kΩ, then R_3 = 10 kΩ

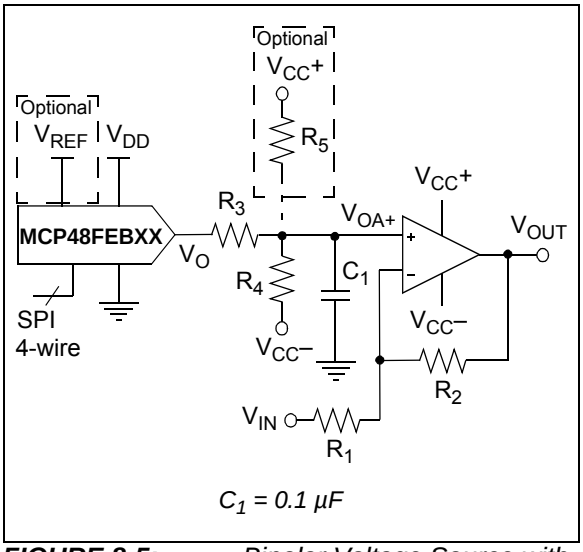


FIGURE 8-5: *Bipolar Voltage Source with Selectable Gain and Offset.*

EQUATION 8-6: V_{OUT}, V_{OA+}, AND V_O CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4 + V_{CC-} \bullet R_5}{R_3 + R_4}$$

$$V_O = \underbrace{V_{OA+} \bullet \left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_{IN} \bullet \left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

EQUATION 8-7: BIPOLAR "WINDOW" DAC USING R_4 AND R_5

Thevenin Equivalent

$$V_{45} = \frac{V_{CC+}R_4 + V_{CC-}R_5}{R_4 + R_5}$$

$$V_{IN+} = \frac{V_{OUT}R_{45} + V_{45}R_3}{R_3 + R_{45}}$$

$$R_{45} = \frac{R_4R_5}{R_4 + R_5}$$

$$V_O = \underbrace{V_{IN+}\left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_A\left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

8.5 Designing a Double-Precision DAC

Figure 8-6 shows an example design of a single-supply voltage output capable of up to 24-bit resolution. This requires two 12-bit DACs. This design is simply a voltage divider with a buffered output.

Double-Precision DAC Example

If a similar application to the one developed in Bipolar DAC Example required a resolution of 1 µV instead of 1 mV and a range of 0V to 4.1V, then 12-bit resolution would not be adequate.

Step 1: Calculate the resolution needed:

4.1V/1 µV = 4.1 x 10^6.
Since 2^{22} = 4.2 x 10^6, 22-bit resolution is desired. Since DNL = ±1.0 LSb, this design can be attempted with the 12-bit DAC.

Step 2: Since DAC1's V_{OUT1} has a resolution of 1 mV, its output only needs to be "pulled" 1/1000 to meet the 1 µV target. Dividing V_{OUT0} by 1000 would allow the application to compensate for DAC1's DNL error.

Step 3: If R_2 is 100Ω, then R_1 needs to be 100 kΩ.

Step 4: The resulting transfer function is shown in the equation of Example 8-8.

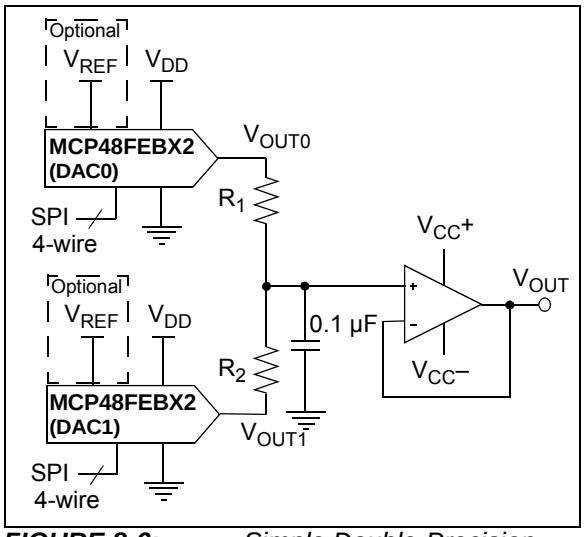


FIGURE 8-6: *Simple Double-Precision DAC using MCP48FEBX2.*

EQUATION 8-8: V_{OUT} CALCULATION

$$V_{OUT} = \frac{V_{OUT0} \bullet R_2 + V_{OUT1} \bullet R_1}{R_1 + R_2}$$

Where:

V_{OUT0} = (V_{REF} • G • DAC0 Register Value)/4096

V_{OUT1} = (V_{REF} • G • DAC1 Register Value)/4096

Gx = Selected Op Amp Gain

8.6 Building Programmable Current Source

Figure 8-7 shows an example of building a programmable current source using a voltage follower. The current sensor resistor is used to convert the DAC voltage output into a digitally-selectable current source.

The smaller R_{SENSE} is, the less power dissipated across it. However, this also reduces the resolution that the current can be controlled.

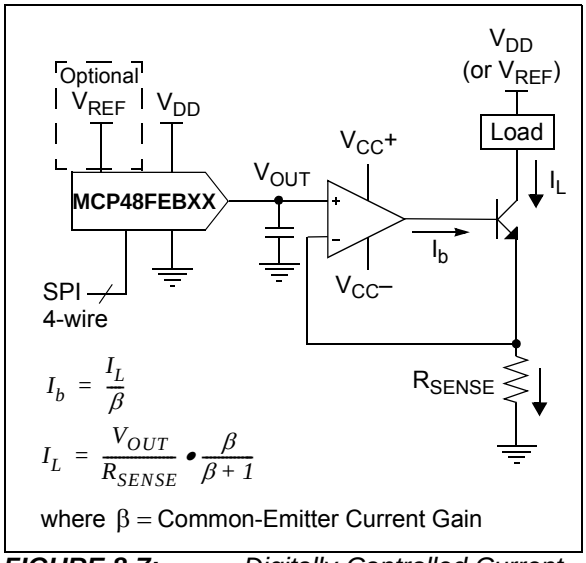


FIGURE 8-7: *Digitally-Controlled Current Source.*

8.7 Serial Interface Communication Times

Table 8-1 shows time/frequency of the supported operations of the SPI serial interface for the different serial interface operational frequencies. This, along with the V_{OUT} output performance (such as slew rate), would be used to determine your application's volatile DAC register update rate.

TABLE 8-1: SERIAL INTERFACE TIMES / FREQUENCIES

Command					# of Bit Clocks (2)	Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second)			Comments
Operation	Code C1	Code C0	HV	Mode (1)		1 MHz	10 MHz	20 MHz (3)	
Write Command	0	0	No(4)	Single	24	41,666	416,666	833,333	
	0	0	No(4)	Continuous	24n	41,666	416,666	833,333	For 10 data words
Read Command (5)	1	1	No(4)	Single	24	41,666	416,666	N.A.	
	1	1	No(4)	Continuous	24n	41,666	416,666	N.A.	For 10 data words
Enable Configuration Bit Command	1	0	Yes	Single	8	125,000	1,250,000	2,500,000	
	1	0	Yes	Continuous	8n	125,000	1,250,000	2,500,000	For 10 data words
Disable Configuration Bit Command	0	1	Yes	Single	8	125,000	1,250,000	2,500,000	
	0	1	Yes	Continuous	8n	125,000	1,250,000	2,500,000	For 10 data words

Note 1: Nonvolatile registers can only use the "Single" mode.

2: "n" indicates the number of times the command operation is to be repeated.

3: `Write` command only.

4: If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated

5: This command is useful to determine when an EEPROM programming cycle has completed.

8.8 Design Considerations

In the design of a system with the MCP48FEBXX devices, the following considerations should be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

8.8.1 POWER SUPPLY CONSIDERATIONS

The typical application will require a bypass capacitor in order to filter high-frequency noise which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-8 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin (V_{DD}) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} should reside on the analog plane.

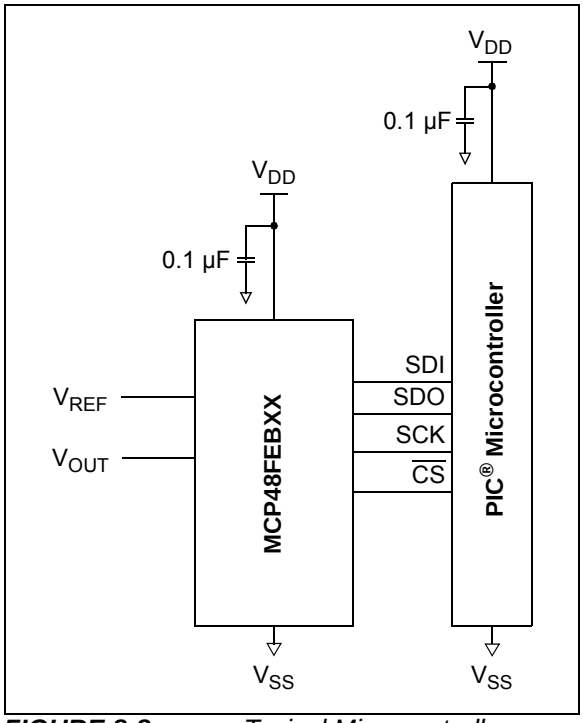


FIGURE 8-8: *Typical Microcontroller Connections.*

8.8.2 LAYOUT CONSIDERATIONS

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **PCB Area Requirements**

8.8.2.1 Noise

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP48FEBXX's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors should be terminated to the analog ground plane.

Note:	Breadboards and wire-wrapped boards are not recommended.

8.8.2.2 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-2 shows the typical package dimensions and area for the different package options.

TABLE 8-2: PACKAGE FOOTPRINT(1)

Package			Package Footprint		
Pins	Type	Code	Dimensions (mm)		Area (mm^2)
			Length	Width	
10	MSOP	UN	3.00	4.90	14.70

Note 1: Does not include recommended land pattern dimensions. Dimensions are typical values.

NOTES:

9.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups. These are:

- Development Tools
- Technical Documentation

9.1 Development Tools

The MCP48FEBXX devices currently do not have any development tools or bond-out boards. Please visit the Device's web product page (Development Tools tab) for the development tools availability after the release of this data sheet.

9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-1 shows some of these documents.

TABLE 9-1: TECHNICAL DOCUMENTATION

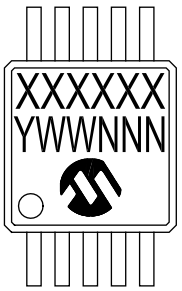
Application Note Number	Title	Literature #
AN1326	Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications	DS01326
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

NOTES:

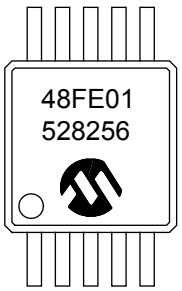
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

10-Lead MSOP



Example



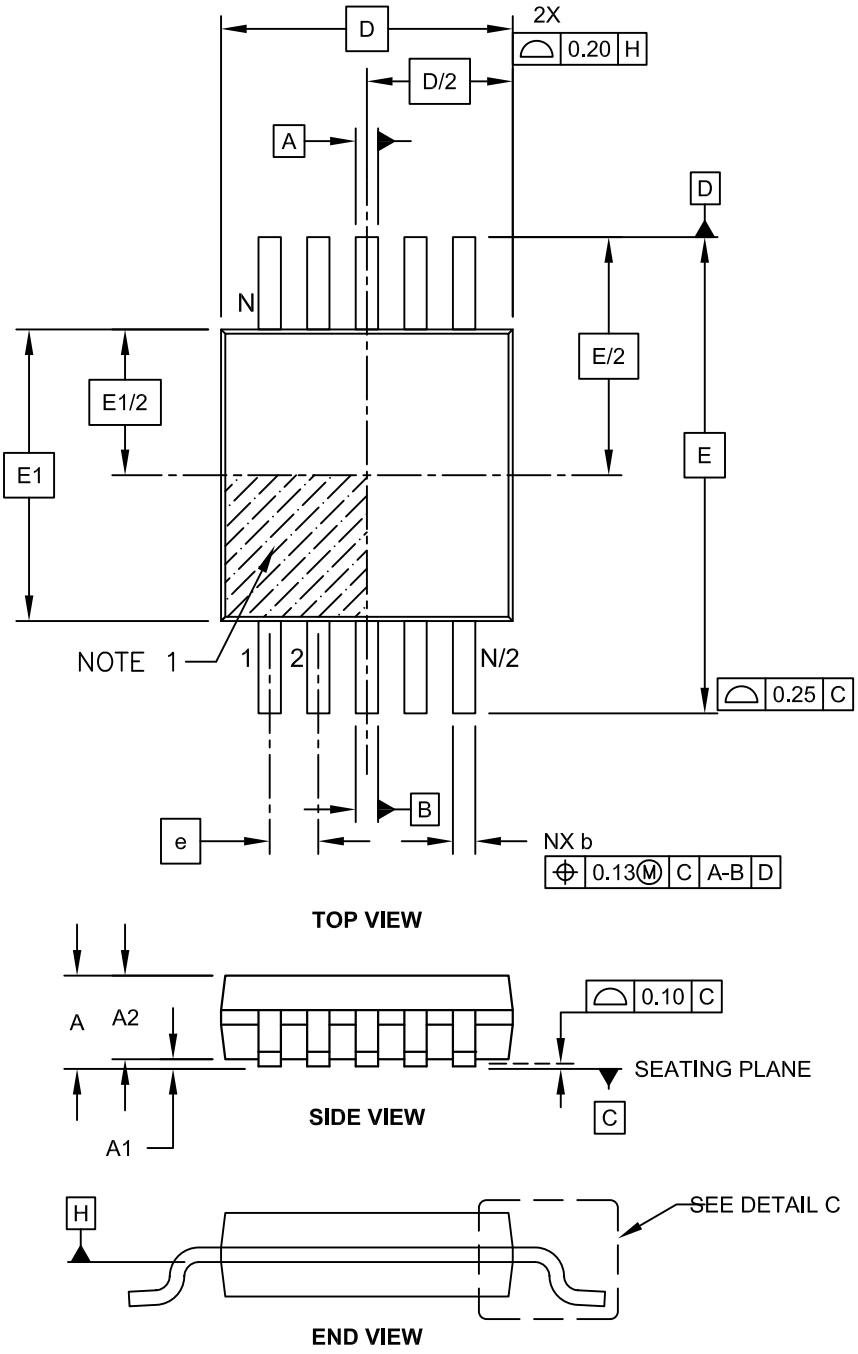
Device Number	Code	Device Number	Code
MCP48FEB01-E/UN	48FE01	MCP48FEB02-E/UN	48FE02
MCP48FEB01T-E/UN	48FE01	MCP48FEB02T-E/UN	48FE02
MCP48FEB11-E/UN	48FE11	MCP48FEB12-E/UN	48FE12
MCP48FEB11T-E/UN	48FE11	MCP48FEB12T-E/UN	48FE12
MCP48FEB21-E/UN	48FE21	MCP48FEB22-E/UN	48FE22
MCP48FEB21T-E/UN	48FE21	MCP48FEB22T-E/UN	48FE22

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

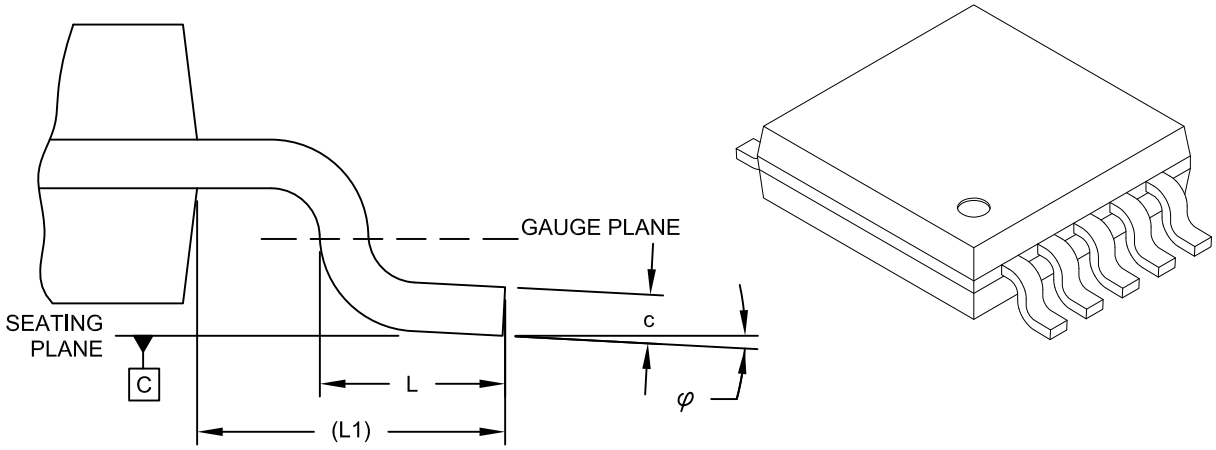
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-021C Sheet 1 of 2

10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.15	-	0.33

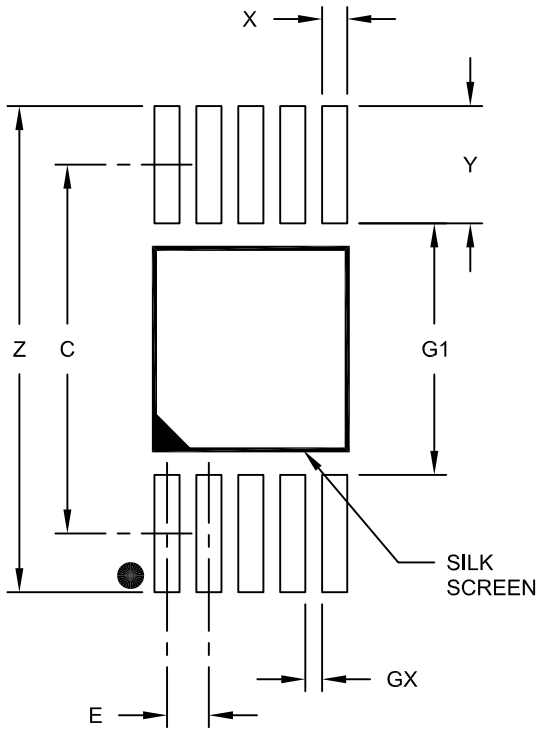
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021C Sheet 2 of 2

10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads	G1	3.00		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021A

APPENDIX A: REVISION HISTORY

Revision B (September 2015)

- Fixed a header/part number typographical error.

Revision A (September 2015)

- Original release of this document.

APPENDIX B: TERMINOLOGY

B.1 Resolution

Resolution is the number of DAC output states that divide the full-scale range. For the 12-bit DAC, the resolution is 2^{12}, meaning the DAC code ranges from 0 to 4095.

Note:	When there are 2^N resistors in the resistor ladder and 2^N tap points, the full-scale DAC register code is the resistor element (1 LSb) from the source reference voltage (V_{DD} or V_{REF}).

B.2 Least Significant Bit (LSb)

This is the voltage difference between two successive codes. For a given output voltage range, it is divided by the resolution of the device (Equation B-1). The range may be V_{DD} (or V_{REF}) to V_{SS} (ideal), the DAC register codes across the linear range of the output driver (Measured 1), or full-scale to zero-scale (Measured 2).

EQUATION B-1: LSb VOLTAGE CALCULATION

Ideal

$$V_{LSb(IDEAL)} = \frac{V_{DD}}{2^N} \text{ or } \frac{V_{REF}}{2^N}$$

Measured 1

$$V_{LSb(Measured)} = \frac{V_{OUT(@4000)} - V_{OUT(@100)}}{(4000 - 100)}$$

Measured 2

$$V_{LSb} = \frac{V_{OUT(@FS)} - V_{OUT(@ZS)}}{2^N - 1}$$

2^N = 4096 (MCP48FEB2X)
= 1024 (MCP48FEB1X)
= 256 (MCP48FEB0X)

B.3 Monotonic Operation

Monotonic operation means that the device's output voltage (V_{OUT}) increases with every 1 code step (LSb) increment (from V_{SS} to the DAC's reference voltage (V_{DD} or V_{REF})).

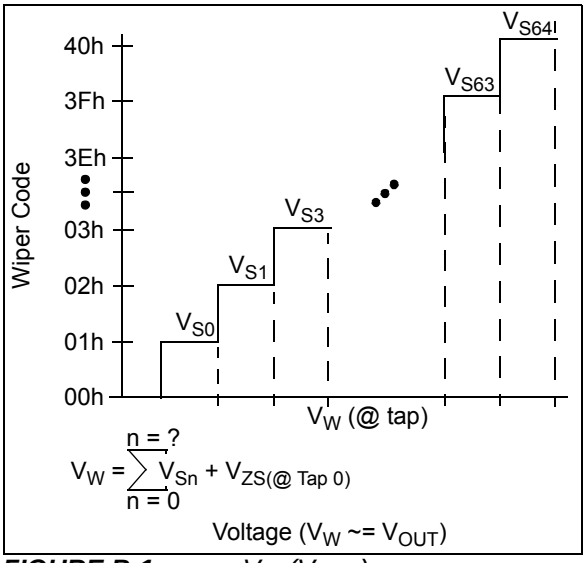


FIGURE B-1: *V_W (V_{OUT}).*

B.4 Full-Scale Error (E_{FS})

The Full-Scale Error (see Figure B-3) is the error on the V_{OUT} pin relative to the expected V_{OUT} voltage (theoretical) for the maximum device DAC register code (code FFFh for 12-bit, code 3FFh for 10-bit, and code FFh for 8-bit) (see Equation B-2). The error is dependent on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{SS}) greater than specified, the full-scale error will be greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

EQUATION B-2: FULL-SCALE ERROR

$$E_{FS} = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS} is expressed in LSb.

$V_{OUT(@FS)}$ = The V_{OUT} voltage when the DAC register code is at full-scale.

$V_{IDEAL(@FS)}$ = The ideal output voltage when the DAC register code is at full-scale.

$V_{LSb(IDEAL)}$ = The theoretical voltage step size.

B.5 Zero-Scale Error (E_{ZS})

The Zero-Scale Error (see Figure B-2) is the difference between the ideal and measured V_{OUT} voltage with the DAC register code equal to 000h (Equation B-3). The error is dependent on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{DD}) greater than specified, the zero-scale error will be greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

EQUATION B-3: ZERO-SCALE ERROR

$$E_{ZS} = \frac{V_{OUT(@ZS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{ZS} is expressed in LSb.

$V_{OUT(@ZS)}$ = The V_{OUT} voltage when the DAC register code is at Zero-scale.

$V_{LSb(IDEAL)}$ = The theoretical voltage step size.

B.6 Total Unadjusted Error (E_T)

The Total Unadjusted Error (E_T) is the difference between the ideal and measured V_{OUT} voltage. Typically, calibration of the output voltage is implemented to improve system performance.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

Equation B-4 shows the Total Unadjusted Error calculation.

EQUATION B-4: TOTAL UNADJUSTED ERROR CALCULATION

$$E_T = \frac{(V_{OUT\_Actual(@code)} - V_{OUT\_Ideal(@Code)})}{V_{LSb(Ideal)}}$$

Where:

E_T is expressed in LSb.

$V_{OUT\_Actual(@code)}$ = The measured DAC output voltage at the specified code.

$V_{OUT\_Ideal(@code)}$ = The calculated DAC output voltage at the specified code. (code * $V_{LSb(Ideal)}$)

$V_{LSb(Ideal)}$ = V_{REF}/# Steps
12-bit = V_{REF}/4096
10-bit = V_{REF}/1024
8-bit = V_{REF}/256

B.7 Offset Error (E_{OS})

The offset error is the delta voltage of the V_{OUT} voltage from the ideal output voltage at the specified code. This code is specified where the output amplifier is in the linear operating range; for the MCP48FEBXX we specify code 100 (decimal). Offset error does not include gain error. Figure B-2 illustrates this.

This error is expressed in mV. Offset error can be negative or positive. The offset error can be calibrated by software in application circuits.

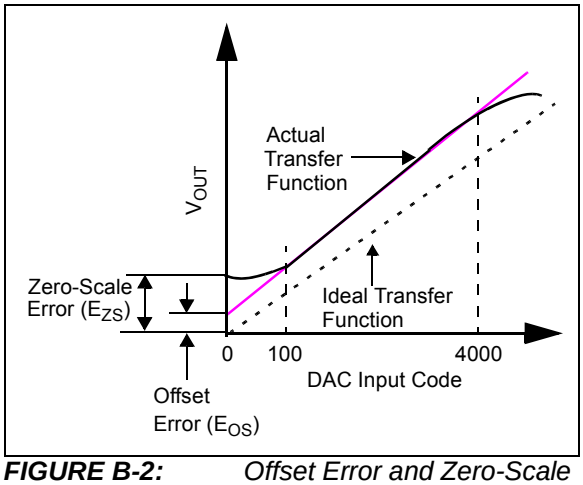


FIGURE B-2: *Offset Error and Zero-Scale Error.*

B.8 Offset Error Drift (E_{OSD})

Offset error drift is the variation in offset error due to a change in ambient temperature. Offset error drift is typically expressed in ppm/°C or µV/°C.

B.9 Gain Error (E_G)

Gain error is a calculation based on the ideal slope using the voltage boundaries for the linear range of the output driver (ex code 100 and code 4000) (see Figure B-3). The gain error calculation nullifies the device's offset error.

Gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed as percent of full-scale range (% of FSR) or in LSb. FSR is the ideal full-scale voltage of the DAC (see Equation B-5).

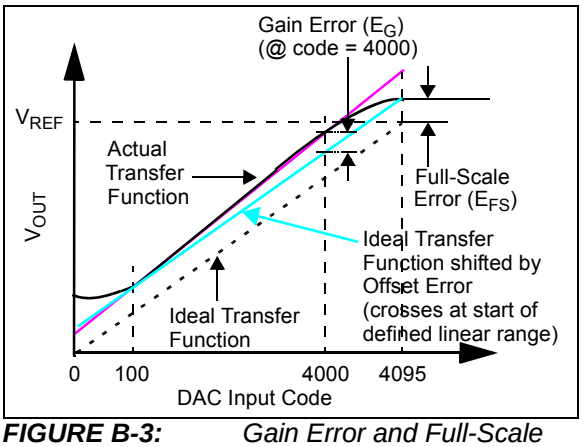


FIGURE B-3: *Gain Error and Full-Scale Error Example.*

EQUATION B-5: EXAMPLE GAIN ERROR

$$E_G = \frac{(V_{OUT(@4000)} - V_{OS} - V_{OUT\_Ideal(@4000)})}{V_{Full\text{-}Scale\ Range}} \cdot 100$$

Where:

E_G is expressed in % of full-scale range (FSR).

$V_{OUT(@4000)}$ = The measured DAC output voltage at the specified code.

$V_{OUT\_Ideal(@4000)}$ = The calculated DAC output voltage at the specified code. (4000 * $V_{LSb(Ideal)}$)

V_{OS} = Measured offset voltage.

$V_{Full\ Scale\ Range}$ = Expected full-scale output value (such as the V_{REF} voltage).

B.10 Gain-Error Drift (E_{GD})

Gain-error drift is the variation in gain error due to a change in ambient temperature. Gain error drift is typically expressed in ppm/°C (of full-scale range).

B.11 Integral Nonlinearity (INL)

The Integral Nonlinearity (INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line) passing through the defined end points of the DAC transfer function (after offset and gain errors have been removed).

In the MCP48FEBXX, INL is calculated using the defined end points, DAC code 100 and code 4000. INL can be expressed as a percentage of full-scale range (FSR) or in LSb. INL is also called Relative Accuracy. Equation B-6 shows how to calculate the INL error in LSb and Figure B-4 shows an example of INL accuracy.

Positive INL means higher V_{OUT} voltage than ideal. Negative INL means lower V_{OUT} voltage than ideal.

EQUATION B-6: INL ERROR

$$E_{INL} = \frac{(V_{OUT} - V_{Calc\_Ideal})}{V_{LSb(Measured)}}$$

Where:

INL is expressed in LSb.

V_{Calc_Ideal} = Code * $V_{LSb(Measured)}$ + V_{OS}

$V_{OUT(Code = n)}$ = The measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4000)} - V_{OUT(100)})/3900$

V_{OS} = Measured offset voltage.

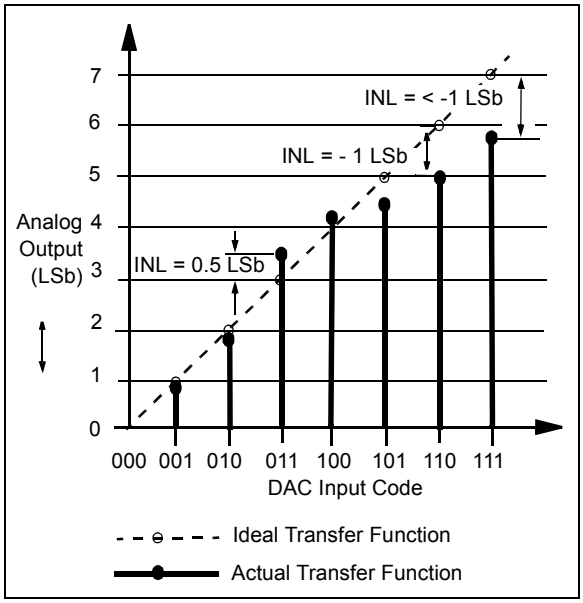


FIGURE B-4: *INL Accuracy.*

B.12 Differential Nonlinearity (DNL)

The Differential Nonlinearity (DNL) error (see Figure B-5) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSb. A DNL error of zero would imply that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC guarantees monotonic output and no missing codes. Equation B-7 shows how to calculate the DNL error between any two adjacent codes in LSb.

EQUATION B-7: DNL ERROR

$$E_{DNL} = \frac{(V_{OUT(code = n+1)} - V_{OUT(code = n)})}{V_{LSb(Measured)}} - 1$$

Where:

DNL is expressed in LSb.

$V_{OUT(Code = n)}$ = The measured DAC output voltage with a given DAC register code.

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4000)} - V_{OUT(100)})/3900$

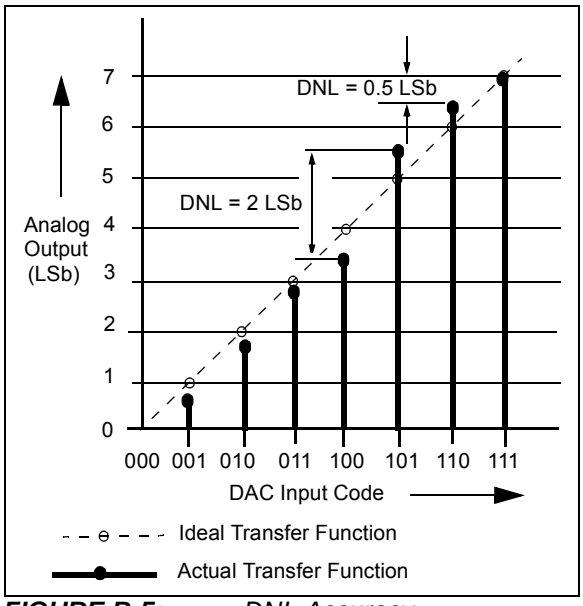


FIGURE B-5: *DNL Accuracy.*

B.13 Settling Time

Settling time is the time delay required for the V_{OUT} voltage to settle into its new output value. This time is measured from the start of code transition to when the V_{OUT} voltage is within the specified accuracy.

In the MCP48FEBXX, the settling time is a measure of the time delay until the V_{OUT} voltage reaches within 0.5 LSb of its final value, when the volatile DAC Register changes from 1/4 to 3/4 of the full-scale range (12-bit device: 400h to C00h).

B.14 Major-Code Transition Glitch

Major-Code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec, and is measured when the digital code is changed by 1 LSb at the major carry transition.

Example: `011...111` to `100...000`
or `100...000` to `011...111`

B.15 Digital Feed-through

Digital feed-through is the glitch that appears at the analog output, caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec, and is measured with a full-scale change on the digital input pins.

Example: all `0`s to all `1`s and vice versa.

The digital feed-through is measured when the DAC is not being written to the output register.

B.16 -3 dB Bandwidth

This is the frequency of the signal at the V_{REF} pin that causes the voltage at the V_{OUT} pin to fall -3 dB value from a static value on the V_{REF} pin. The output decreases due to the RC characteristics of the resistor ladder and the characteristics of the output buffer.

B.17 Power-Supply Sensitivity (PSS)

PSS indicates how the output of the DAC is affected by changes in the supply voltage. PSS is the ratio of the change in V_{OUT} to a change in V_{DD} for mid-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied from 5.5V to 2.7V as a step (V_{REF} voltage held constant), and expressed in %/%, which is the % change of the DAC output voltage with respect to the % change of the V_{DD} voltage.

EQUATION B-8: PSS CALCULATION

$$PSS = \frac{\frac{V_{OUT(@5.5V)} - V_{OUT(@2.7V)}}{V_{OUT(@5.5V)}}}{\frac{(5.5V - 2.7V)}{5.5V}}$$

Where:

PSS is expressed in %/%.

$V_{OUT(@5.5V)}$ = The measured DAC output voltage with V_{DD} = 5.5V.

$V_{OUT(@2.7V)}$ = The measured DAC output voltage with V_{DD} = 2.7V.

B.18 Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied ± 10% (V_{REF} voltage held constant), and expressed in dB or µV/V.

B.19 V_{OUT} Temperature Coefficient

The V_{OUT} Temperature Coefficient quantifies the error in the resistor ladder's resistance ratio (DAC Register code value) and Output Buffer due to temperature drift.

B.20 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (Nominal output voltage V_{OUT}) due to temperature drift. For a DAC this error is typically not an issue due to the ratiometric aspect of the output.

B.21 Noise Spectral Density

Noise spectral density is a measurement of the device's internally-generated random noise, and is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to the mid-scale value and measuring the noise at the V_{OUT} pin. It is measured in nV/√Hz.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[1]	X	— /XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP48FEB01:	Single-Channel 8-Bit NV DAC with External + Internal References
	MCP48FEB02:	Dual-Channel 8-Bit NV DAC with External + Internal References
	MCP48FEB11:	Single-Channel 10-Bit NV DAC with External + Internal References
	MCP48FEB12:	Dual-Channel 10-Bit NV DAC with External + Internal References
	MCP48FEB21:	Single-Channel 12-Bit NV DAC with External + Internal References
	MCP48FEB22:	Dual-Channel 12-Bit NV DAC with External + Internal References
Tape and Reel:	T =	Tape and Reel[1]
	Blank =	Tube
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	UN =	Plastic Micro Small Outline (MSOP), 10-Lead

Examples:

a) MCP48FEB01-E/UN:	8-bit V_{OUT} resolution, Single Channel, Tube, Extended Temperature., 10-Lead MSOP Package
b) MCP48FEB01T-E/UN:	8-bit V_{OUT} resolution, Single Channel, Tape and Reel, Extended Temperature, 10-Lead MSOP Package
a) MCP48FEB11-E/UN:	10-bit V_{OUT} resolution, Single Channel, Tube, Extended Temperature, 10-Lead MSOP Package
b) MCP48FEB11T-E/UN:	10-bit V_{OUT} resolution, Single Channel, Tape and Reel, Extended Temperature, 10-Lead MSOP Package
a) MCP48FEB21-E/UN:	12-bit V_{OUT} resolution, Single Channel, Tube, Extended Temperature, 10-Lead MSOP Package
b) MCP48FEB21T-E/UN:	12-bit V_{OUT} resolution, Single Channel, Tape and Reel, Extended Temperature, 10-Lead MSOP Package
a) MCP48FEB22-E/UN:	12-bit V_{OUT} resolution, Dual Channel, Tube, Extended Temperature, 10-Lead MSOP Package
b) MCP48FEB22T-E/UN:	12-bit V_{OUT} resolution, Dual Channel, Tape and Reel, Extended Temperature, 10-Lead MSOP Package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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ISBN: 978-1-63277-828-4

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07/14/15