HV7350

8-Channel High-Speed ±60V ±1A Ultrasound RTZ Pulser

Features

- HVCMOS® Technology for High Performance
- High-density Integrated Ultrasound Transmitter
- 0V to ±60V Output Voltage
- ±1A Source and Sink Current in Pulse Mode
- ±1A Source and Sink Current in Return-to-Zero (RTZ) Mode
- Up to 20 MHz Operating Frequency
- Matched Delay Times
- Optional Clock Realignment
- 3.3V CMOS Logic Interface and Reference
- +3.3V Low-voltage Supply for V_{DD}
- Built-in Linear Regulators for Floating Gate Drivers
- Built-in Output Drain Diodes and Bleed Resistors

Applications

- Portable Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Pulse Waveform Generator

General Description

The HV7350 is an 8-channel monolithic high-voltage high-speed pulse generator with built-in fast return to zero-damping FETs. This high-voltage and high-speed integrated circuit is designed for portable medical ultrasound imaging system.

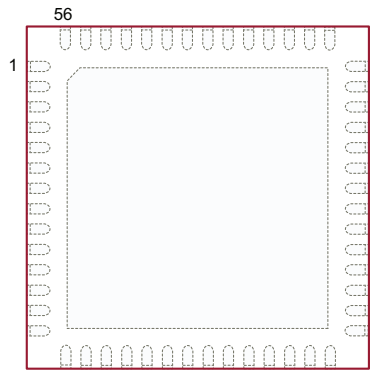
The HV7350 consists of a controller logic interface circuit, level translators, MOSFET gate drives, and high-current power P-channel and N-channel MOSFETs as the output stage for each channel.

The output peak currents of each channel are guaranteed to be over ±1A with up to ±60V pulse swings as well as Return-to-Zero mode. The gate drivers for the output MOSFETs are powered by built-in linear 5V regulators referenced to V_{PP} and V_{NN}. This direct coupling topology of the gate drivers not only saves four floating voltage supplies or AC coupling capacitors per channel but also makes the PCB layout smaller and easier.

An input clock pin is available to realign all the logic input control lines to a master clock. Precise logic timing is always essential in any ultrasound systems.

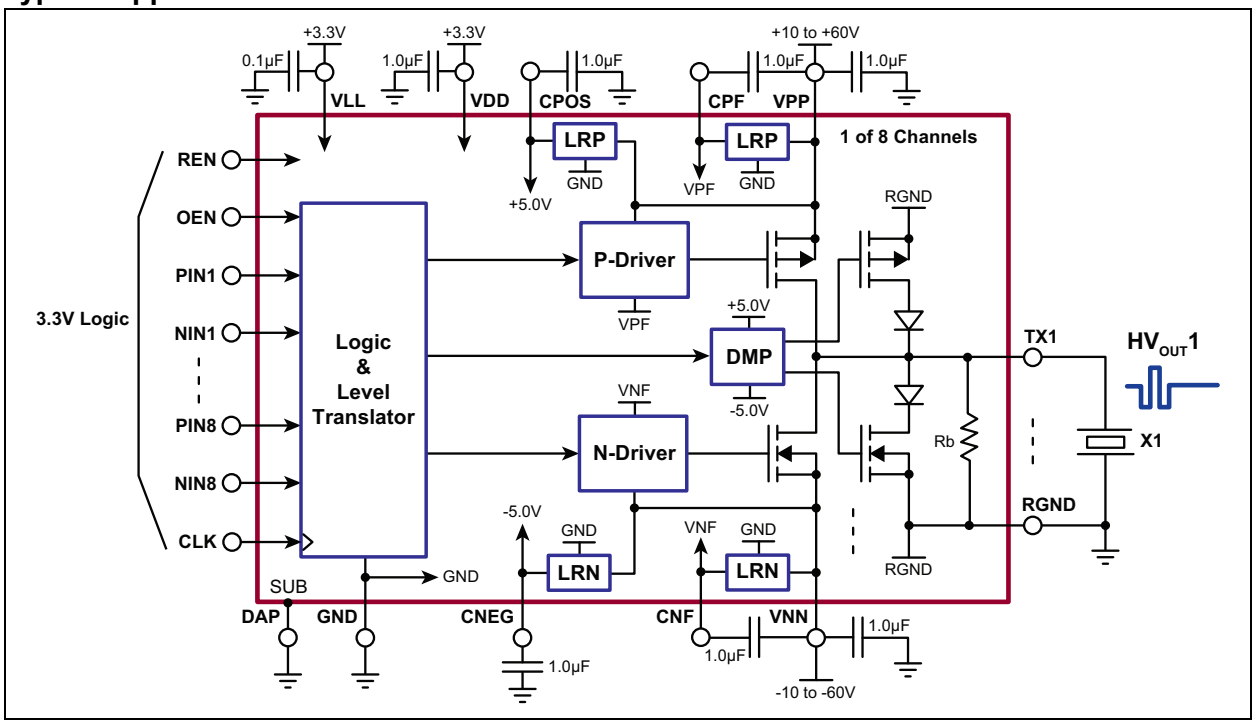
Package Type

56-lead (8 X 8) QFN
(Top view)



See Table 2-1 for pin information.

Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

GND and Substrate Voltage, VSUB 0V
Positive Logic Supply, V_{LL} ..... –0.5V to +5.5V
Positive Logic and Level Translator Supply, V_{DD} ..... –0.5V to +5.5V
Positive Level Translator Decoupling Pin, C_{POS} to GND ..... –0.5V to +5.5V
Negative Level Translator Decoupling Pin, C_{NEG} to GND ..... +0.5V to –5.5V
Positive Floating Gate Driver Decoupling Pin, V_{PP}–C_{PF} ..... –0.5V to +5.5V
Floating Gate Driver Decoupling Pin, C_{NF}–V_{NN} ..... –0.5V to +5.5V
Differential High-voltage Supply, V_{PP}–V_{NN} ..... +130V
High-voltage Positive Supply, V_{PP} ..... –0.5V to +65V
High-voltage Negative Supply, V_{NN} ..... +0.5V to –65V
All Logic Input CLK, PIN_X, NIN_X, OEN and REN Voltages ..... –0.5V to +5.5V
Operating Junction Temperature, T_J ..... –40°C to +125°C
Storage Temperature, T_S ..... –65°C to +150°C
ESD Rating (**Note 1**) ..... ESD Sensitive

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD sensitive. Handling precautions are recommended.

OPERATING SUPPLY VOLTAGES AND CURRENT (EIGHT ACTIVE CHANNELS)

Electrical Specifications: V_{LL} = +3.3V, V_{DD} = +3.3V, V_{PP} = +60V, V_{NN} = –60V, V_{CLK} = +3.3V, T_A = 25°C unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Voltage Supply	V_{DD}	2.97	3.3	5.2	V	
V_{DD} UVLO	$UVLO_{DD}$	2.3	2.6	2.8	V	
Logic Voltage Reference	V_{LL}	2.5	3.3	5	V	
V_{LL} UVLO	$UVLO_{LL}$	1.3	1.55	1.7	V	
Positive High-voltage Supply	V_{PP}	+10	—	+60	V	
Negative High-voltage Supply	V_{NN}	–60	—	–10	V	
V_{LL} Current	I_{LLQ}	—	8	—	μA	OEN = REN = 0
V_{DD} Current	I_{DDQ}	—	1	—		
V_{PP} Current	I_{PPQ}	—	5	10		
V_{NN} Current	I_{NNQ}	—	5	10		
V_{LL} Current	I_{LLEN}	—	13	20	μA	OEN = REN = 1 5 ms after f = 0 MHz
V_{DD} Current	I_{DDEN}	—	480	700		
V_{PP} Current	I_{PPEN}	—	220	350		
V_{NN} Current	I_{NNEN}	—	300	400		
V_{DD} Current	I_{DDCW}	—	2.3	—	mA	f = 5 MHz, continuous, no loads, for calculation reference only
V_{PP} Current	I_{PPCW}	—	80	—		
V_{NN} Current	I_{NNCW}	—	80	—		
VLL Current	$I_{LL,CLK}$	—	33	—	μA	f_{CLK} = 10 MHz, PIN = NIN = 0

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{LL} = +3.3V, V_{DD} = +3.3V, V_{PP} = +60V,V_{NN} = –60V, V_{CLK} = +3.3V, T_A = 25°C unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
PULSER P-CHANNEL MOSFET						
Output Saturation Current	I_{OUT}	1	1.5	—	A	
Channel Resistance	R_{ON}	—	13.2	—	Ω	I_{SD} = 100 mA
PULSER P-CHANNEL MOSFET						
Output Saturation Current	I_{OUT}	1	1.5	—	A	
Channel Resistance	R_{ON}	—	8	—	Ω	I_{SD} = 100 mA
DAMPING P-CHANNEL MOSFET						
Output Saturation Current	I_{OUT}	1	1.5	—	A	
Channel Resistance	R_{ON}	—	13	—	Ω	I_{SD} = 100 mA
DAMPING N-CHANNEL MOSFET						
Output Saturation Current	I_{OUT}	1	1.5	—	A	
Channel Resistance	R_{ON}	—	9	—	Ω	I_{SD} = 100 mA
LOGIC INPUT						
Input Logic High Voltage	V_{IH}	0.7 • V_{LL}	—	V_{LL}	V	V_{LL} = 2.5V to 3.3V
		0.8 • V_{LL}	—			V_{LL} = 5V
Input Logic Low Voltage	V_{IL}	0	—	0.3 • V_{LL}	V	V_{LL} = 2.5V to 3.3V
			—	0.2 • V_{LL}		V_{LL} = 5V
Input Logic High Current	I_{IH}	—	—	10	µA	
Input Logic Low Current	I_{IL}	–10	—	—	µA	
Input Logic Capacitance	C_{IN}	—	—	5	pF	
MOSFET DRAIN BLEED RESISTOR						
Output Bleed Resistance	$R_{B1~8}$	12	17	25	kΩ	
Bleed Resistors Power Limit	$P_{RB1~8}$	—	—	50	mW	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{LL} = +3.3V, V_{DD} = +3.3V, V_{PP} = +60V, V_{NN} = –60V, V_{CLK} = +3.3V, T_A = 25°C unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Output Rise Time	t_r	—	30	—	ns	330 pF//2.5 kΩ load 10%–90%
Output Fall Time	t_f	—	30	—	ns	
Enable Time	t_{EN}	—	300	500	µs	Cap value (See **Typical Application Circuit**.), OEN = REN
Disable Time	t_{DIS}	—	2.8	10	µs	
Delay Time on PIN_X Rise	t_{d1}	—	12	—	ns	1 Ω resistor load, D% < 1% (See **Timing Waveforms**.) 50% inputs to 50% T_X current
Delay Time on NIN_X Rise	t_{d2}	—	12	—		
Delay Time on Damping Rise	t_{d3}	—	12	—		
Delay Time on Damping Fall	t_{d4}	—	12	—		
Delay Time on CLK Rise	t_{dc}	—	9	—		
Delay Time Matching	Δt_{DELAY}	—	±3	—	ns	P to N, channel to channel
Delay Jitter on Rise or Fall	t_J	—	30	—	ps	V_{PP}/V_{NN} = +/–25V, input t_r 50% to HV_{OUT} t_r or t_f 50%, with 330 pF//2.5 kΩ load
RTZ FETs Drain Diode t_{rr}	t_{rr}	—	25	—	ns	I_F = 1A, I_R = 1A, R_L = 10Ω

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: V_{LL} = +3.3V, V_{DD} = +3.3V, V_{PP} = +60V, V_{NN} = –60V, V_{CLK} = +3.3V, T_A = 25°C unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Retiming Clock Frequency	f_{CLK}	10	220	—	MHz	
Retiming Clock Rise and Fall Times	t_{rc}, t_{fc}	—	0.5	5	ns	
Set-up Time, PIN/NIN to CLK	t_{SU}	2	—	—	ns	
Hold time, CLK to PIN/NIN	t_H	1	—	—	ns	
Clock Time Low	t_{CLK_LO}	2	—	100	ns	CLK input must have at least one pulse before PIN and NIN inputs are not zero. Be sure to return inputs to zero before stopping clock.
Clock Time High	t_{CLK_HI}	2	—	100	ns	
Clock Recognition Time	t_{CLK_REC}	—	2	—	ns	
Clock Release Time	t_{CLK_RLS}	150	300	800	ns	
Output Frequency Range	f_{OUT}	—	—	20	MHz	100Ω resistor load
Second Harmonic Distortion	HD2	—	–40	—	dB	
Output Capacitance	C_{OSS}	—	50	—	pF	V_{DS} = 25V, f = 1 MHz of T_X pin total

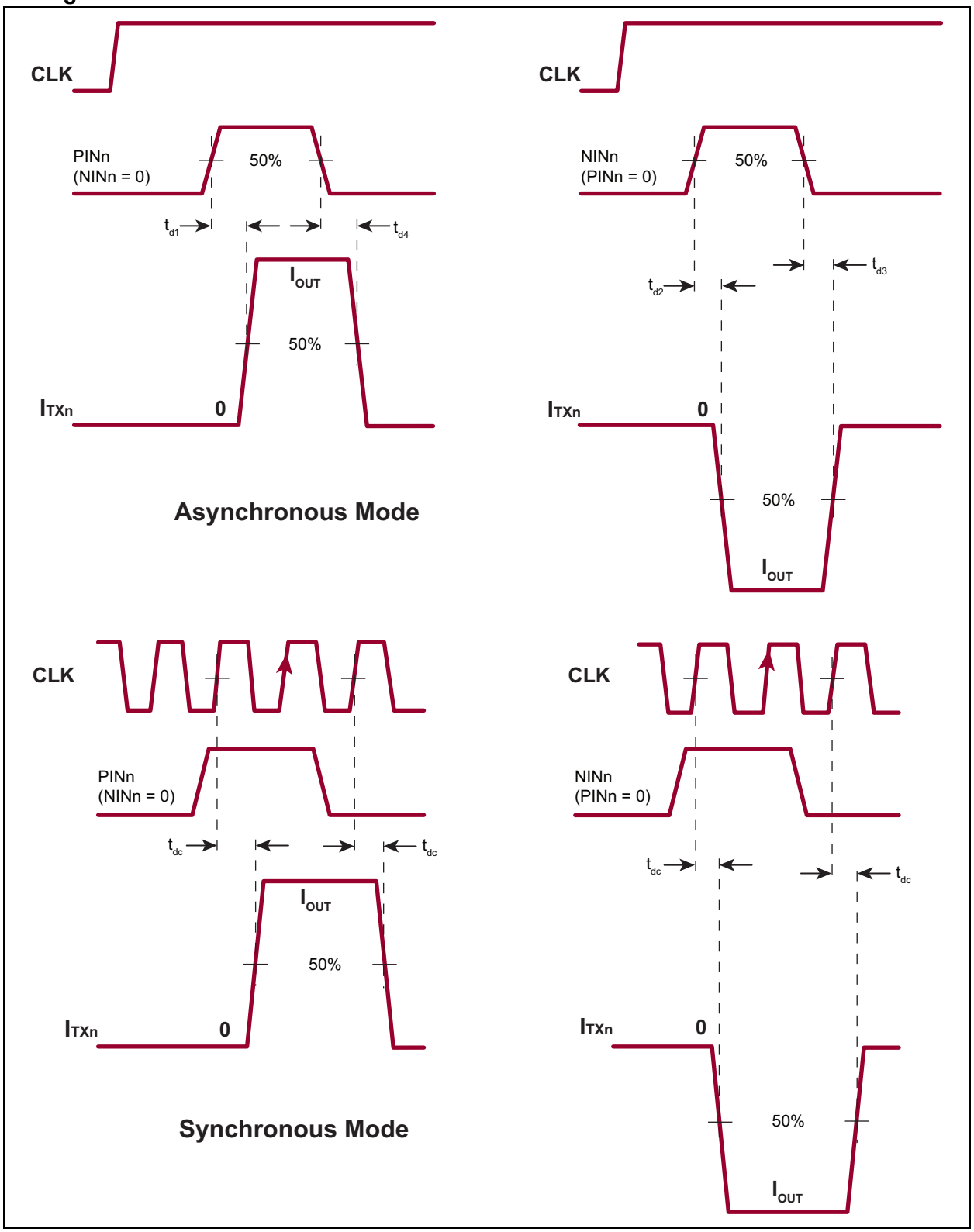
TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–40	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
56-lead (8 X 8) QFN	θ_{JA}	—	21	—	°C/W	

LOGIC CONTROL TABLE

MODE	LOGIC INPUTS				TX_N, OUTPUT		
	OEN	CLK	PIN_X	NINX	VPP	VNN	RGND
Asynchronous Mode Output Change on PIN/NIN	1	VLL	0	0	OFF	OFF	ON
	1	VLL	1	0	ON	OFF	OFF
	1	VLL	0	1	OFF	ON	OFF
	1	VLL	1	1	OFF	OFF	OFF
Synchronous Mode Output Change at Retiming Clock (CLK) Rising Edge, registered by PIN/NIN	1	⎍	0	0	OFF	OFF	ON
	1	⎍	1	0	ON	OFF	OFF
	1	⎍	0	1	OFF	ON	OFF
	1	⎍	1	1	OFF	OFF	OFF
Disabled	0	X	X	X	OFF	OFF	OFF

Timing Waveforms



2.0 PAD DESCRIPTION

Table 2-1 details the description of pads in HV7350.
Refer to **Package Type** for the location of pins.

TABLE 2-1: PAD FUNCTION TABLE

Pin Number	Pin Name	Description
1	PIN2	Input logic control of high-voltage output P-FET for Channel 2; High = on; Low = off (See **Logic Control Table**.)
2	NIN2	Input logic control of high-voltage output N-FET for Channel 2; High = on; Low = off (See **Logic Control Table**.)
3	PIN3	Input logic control of high-voltage output P-FET for Channel 3; High = on; Low = off (See **Logic Control Table**.)
4	NIN3	Input logic control of high-voltage output N-FET for Channel 3; High = on; Low = off (See **Logic Control Table**.)
5	PIN4	Input logic control of high-voltage output P-FET for Channel 4; High = on; Low = off (See **Logic Control Table**.)
6	NIN4	Input logic control of high-voltage output N-FET for Channel 4; High = on; Low = off (See **Logic Control Table**.)
7	OEN	Output enable; High = on; Low = off (See **Logic Control Table**.)
8	REN	Built-in positive and negative 5V voltage regulators enable; High = on; Low = off If REN = 0, four isolated 5V power supplies may provide, as external supplies, for the VPP to CPF, CNF to VNN, CPOS to GND and GND to CNEG pins. Note that between VPP to CPF and CNF to VNN, two must be floating supplies. (See **Logic Control Table**.)
9	PIN5	Input logic control of high-voltage output P-FET for Channel 5; High = on; Low = off (See **Logic Control Table**.)
10	NIN5	Input logic control of high-voltage output N-FET for Channel 5; High = on; Low = off (See **Logic Control Table**.)
11	PIN6	Input logic control of high-voltage output P-FET for Channel 6; High = on; Low = off (See **Logic Control Table**.)
12	NIN6	Input logic control of high-voltage output N-FET for Channel 6; High = on; Low = off (See **Logic Control Table**.)
13	PIN7	Input logic control of high-voltage output P-FET for Channel 7; High = on; Low = off (See **Logic Control Table**.)
14	NIN7	Input logic control of high-voltage output N-FET for Channel 7; High = on; Low = off (See **Logic Control Table**.)
15	PIN8	Input logic control of high-voltage output P-FET for Channel 8; High = on; Low = off (See **Logic Control Table**.)
16	NIN8	Input logic control of high-voltage output N-FET for Channel 8; High = on; Low = off (See **Logic Control Table**.)
17	VLL	Logic supply voltage and reference input (+3.3V)
18	GND	Logic and circuit return ground (0V)
19	VDD	Positive voltage power supply (+3.3V)
20	VPP	Positive high-voltage power supply (+10V to +60V)
21	VPP	
22	VPP	
23	CPF	Built-in linear voltage VPF regulator output decoupling capacitor pin, 1 uF from VPP to CPF for every CPF pin
24	CNF	Built-in linear voltage VNF regulator output decoupling capacitor pin, 1 uF from CNF to VNN for every CNF pin
25	VNN	Negative high-voltage power supply (–10V to –60V)
26	VNN	
27	VNN	
28	TX8	T_X pulser Channel 8 output
29	RGND	Damping ground and bleed resistors common return ground

TABLE 2-1: PAD FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
30	TX7	T_X pulser Channel 7 output
31	RGND	Damping ground and bleed resistors common return ground
32	TX6	T_X pulser Channel 6 output
33	RGND	Damping ground and bleed resistors common return ground
34	TX5	T_X pulser Channel 5 output
35	CNEG	Built-in linear voltage –5V regulator output decoupling capacitor pin, 1 uF from CNEG to GND
36	CPOS	Built-in linear voltage +5V regulator output decoupling capacitor pin, 1 uF from CPOS to GND
37	TX4	T_X pulser Channel 4 output
38	RGND	Damping ground and bleed resistors common return ground
39	TX3	T_X pulser Channel 3 output
40	RGND	Damping ground and bleed resistors common return ground
41	TX2	T_X pulser Channel 2 output
42	RGND	Damping ground and bleed resistors common return ground
43	TX1	T_X pulser Channel 1 output
44	VNN	Negative high-voltage power supply (–10V to –60V)
45	VNN	
46	VNN	
47	CNF	Built-in linear voltage VNF regulator output decoupling capacitor pin, 1 uF from CNF to VNN for every CNF pin
48	CPF	Built-in linear voltage VPF regulator output decoupling capacitor pin, 1 uF from VPP to CPF for every CPF pin
49	VPP	Positive high-voltage power supply (+10V to +60V)
50	VPP	
51	VPP	
52	VDD	Positive voltage power supply (+3.3V)
53	GND	Logic and circuit return ground (0V)
54	CLK	Retiming register clock input. Connect to VLL to disable the retiming function.
55	PIN1	Input logic control of high-voltage output P-FET for Channel 1; High = on; Low = off (See **Logic Control Table**.)
56	NIN1	Input logic control of high-voltage output N-FET for Channel 1; High = on; Low = off (See **Logic Control Table**.)
VSUB (Thermal Pad)		Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to GND (0V) externally.

3.0 FUNCTIONAL DESCRIPTION

Follow the steps below to power up and power down the HV7350:

POWER-UP AND POWER-DOWN SEQUENCE (Note 1)

Power-Up		Power-Down	
Step	**Description**	**Step**	**Description**
1	V_{LL} with logic signal low	1	All logic signals go to low
2	V_{DD}	2	V_{PP} and V_{NN}
3	REN = 1 (external supplies on)	3	REN = 0 (external supplies off)
4	V_{PP} and V_{NN}	4	V_{DD}
5	Logic control signals active	5	V_{LL}

Note 1: Powering up or down in any arbitrary sequence will not damage the device. The power-up sequence and power-down sequence are only recommended to minimize possible inrush current.

OUTPUT CURRENT AND R_{ON} (Note 1, Note 4)

I_{SC} [2]	R_{onP}	R_{onN}	I_{DMP} [3]	R_{onDP}	R_{onDN}
1.5A	13Ω	6.5Ω	1.5A	13Ω	8Ω

Note 1: V_{PP}/V_{NN} = +/-60V; V_{DD} = +3.3V; REN = 1

2: I_{SC} is current into 1Ω to GND.

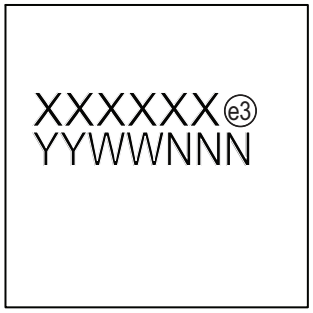
3: I_{DMP} is current from +/–30V connected to T_X pin.

4: Maximum pulse width for current measurement on T_X pin is 20 ns.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

56-lead QFN



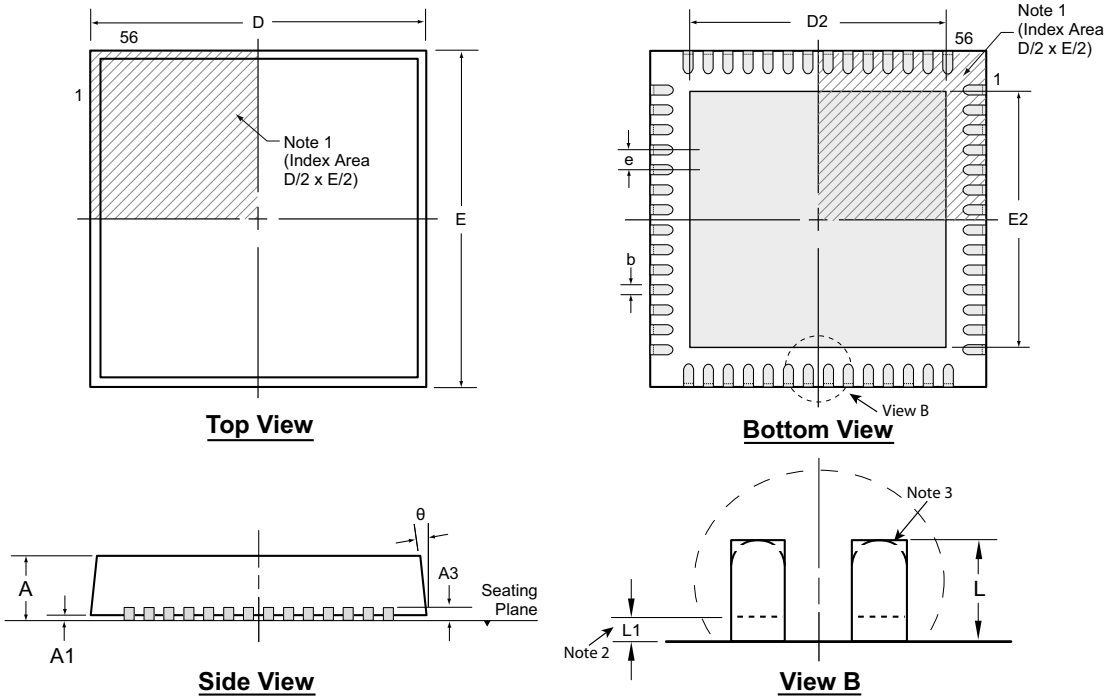
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

56-Lead QFN Package Outline (K6)

8.00x8.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	7.85*	2.75	7.85*	2.75	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	8.00	5.70	8.00	5.70		0.40	-	-
	MAX	1.00	0.05		0.30	8.15*	6.70†	8.15*	6.70†		0.50	0.15	14°

JEDEC Registration MO-220, Variation VLLD-2, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2016)

- Converted Supertex Doc# DSFP-HV7350 to Microchip DS20005627A
- Changed the packaging quantity of 56-lead QFN M937 from 2000/Reel to 3000/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV7350	=	8-Channel High-Speed ±60V ±1A Ultrasound RTZ Pulser
Package:	K6	=	56-lead VQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	250/Tray for a K6 Package
	M937	=	3000/Reel for a K6 Package

Examples:

a) HV7350K6-G: 8-Channel High-Speed ±60V ±1A Ultrasound RTZ Pulser, 56-lead VQFN, 250/Tray

b) HV7350K6-G-M937: 8-Channel High-Speed ±60V ±1A Ultrasound RTZ Pulser, 56-lead VQFN, 3000/Reel

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Japan - Tokyo
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Korea - Daegu
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Fax: 82-53-744-4302

Korea - Seoul
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Malaysia - Kuala Lumpur
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Malaysia - Penang
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