TC6320

N-Channel and P-Channel Enhancement-Mode MOSFET Pair

Features

- Integrated Gate-to-source Resistor
- Integrated Gate-to-source Zener Diode
- Low Threshold
- Low On-resistance
- Low Input Capacitance
- Fast Switching Speeds
- Free from Secondary Breakdown
- Low Input and Output Leakage
- Independent Electrically Isolated N-channel and P-channel

Applications

- High-voltage Pulsers
- Amplifiers
- Buffers
- Piezoelectric Transducer Drivers
- General Purpose Line Drivers
- Logic-level Interfaces

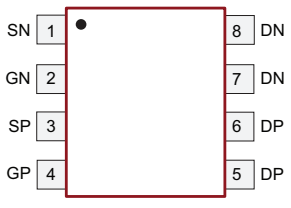
General Description

The TC6320 consists of high-voltage, low-threshold N-channel and P-channel MOSFETs in 8-lead SOIC and DFN packages. Both MOSFETs have integrated gate-to-source resistors and gate-to-source Zener diode clamps which are desired for high-voltage pulser applications. It is a complimentary, high-speed, high-voltage, gate-clamped N-channel and P-channel MOSFET pair, which utilizes an advanced vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

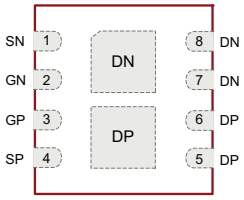
Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

Package Types

8-lead SOIC
(Top view)

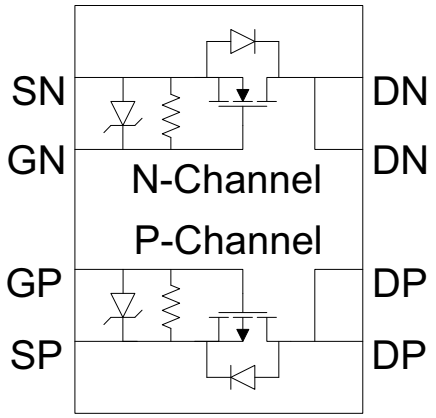


5-lead DFN
(Top view)

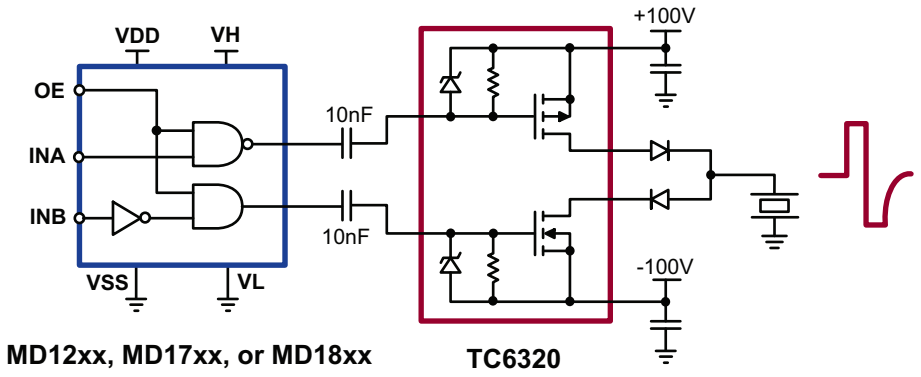


See Table 2-1 and Table 2-2 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-source Voltage ..... BV_{DSS}
Drain-to-gate Voltage ..... BV_{DGS}
Operating Ambient Temperature, T_A ..... –55°C to +150°C
Storage Temperature, T_S ..... –55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = T_J = 25°C$ unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
DC PARAMETER (Note 1 unless otherwise specified)						
Drain-to-source Breakdown Voltage	BV_{DSS}	200	—	—	V	V_{GS} = 0V, I_D = 2 mA
Gate Threshold Voltage	$V_{GS(th)}$	1	—	2	V	$V_{GS} = V_{DS}$, I_D = 1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	–4.5	mV/°C	$V_{GS} = V_{DS}$, I_D = 1 mA (Note 2)
Gate-to-source Shunt Resistor	R_{GS}	10	—	50	kΩ	I_{GS} = 100 µA
Gate-to-Source Zener Voltage	VZ_{GS}	13.2	—	25	V	I_{GS} = 2 mA
Zero-gate Voltage Drain Current	I_{DSS}	—	—	10	µA	V_{DS} = Maximum rating, V_{GS} = 0V
		—	—	1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (Note 2)
On-state Drain Current	$I_{D(ON)}$	1	—	—	A	V_{GS} = 4.5V, V_{DS} = 25V
		2	—	—		V_{GS} = 10V, V_{DS} = 25V
Static Drain-to-source On-state Resistance	$R_{DS(ON)}$	—	—	8	Ω	V_{GS} = 4.5V, I_D = 150 mA
		—	—	7		V_{GS} = 10V, I_D = 1A
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1	%/°C	V_{GS} = 4.5V, I_D = 150 mA (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	G_{FS}	400	—	—	mmho	V_{DS} = 25V, I_D = 500 mA
Input Capacitance	C_{ISS}	—	—	110	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	—	60	pF	
Reverse Transfer Capacitance	C_{RSS}	—	—	23	pF	
Turn-on Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = 25V, I_D = 1A, R_{GEN} = 25Ω
Rise Time	t_r	—	—	15	ns	
Turn-off Delay Time	$t_{d(OFF)}$	—	—	20	ns	
Fall Time	t_f	—	—	15	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	1.8	V	V_{GS} = 0V, I_{SD} = 500 mA (Note 1)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = 500 mA (Note 2)

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

P-CHANNEL ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = T_J = 25°C$ unless otherwise specified.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
DC PARAMETER (Note 1 unless otherwise specified)						
Drain-to-source Breakdown Voltage	BV_{DSS}	–200	—	—	V	V_{GS} = 0V, I_D = –2 mA
Gate Threshold Voltage	$V_{GS(th)}$	–1	—	–2.4	V	$V_{GS} = V_{DS}$, I_D = –1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	4.5	mV/°C	$V_{GS} = V_{DS}$, I_D = –1 mA (**Note 2**)
Gate-to-source Shunt Resistor	R_{GS}	10	—	50	kΩ	I_{GS} = 100 µA
Gate-to-Source Zener Voltage	VZ_{GS}	13.2	—	25	V	I_{GS} = –2 mA
Zero-gate Voltage Drain Current	I_{DSS}	—	—	–10	µA	V_{DS} = Maximum rating, V_{GS} = 0V
		—	—	–1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (**Note 2**)
On-state Drain Current	$I_{D(ON)}$	–1	—	—	A	V_{GS} = –4.5V, V_{DS} = –25V
		–2	—	—		V_{GS} = –10V, V_{DS} = –25V
Static Drain-to-source On-state Resistance	$R_{DS(ON)}$	—	—	10	Ω	V_{GS} = –4.5V, I_D = –150 mA
		—	—	8		V_{GS} = –10V, I_D = –1A
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1	%/°C	V_{GS} = –10V, I_D = –200 mA (**Note 2**)
AC PARAMETER (Note 2)						
Forward Transconductance	G_{FS}	400	—	—	mmho	V_{DS} = –25V, I_D = –500 mA
Input Capacitance	C_{ISS}	—	—	200	pF	V_{GS} = 0V, V_{DS} = –25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	—	55	pF	
Reverse Transfer Capacitance	C_{RSS}	—	—	30	pF	
Turn-on Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = –25V, I_D = –1A, R_{GEN} = 25Ω
Rise Time	t_r	—	—	15	ns	
Turn-off Delay Time	$t_{d(OFF)}$	—	—	20	ns	
Fall Time	t_f	—	—	15	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	–1.8	V	V_{GS} = 0V, I_{SD} = –500 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = –500 mA (**Note 2**)

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, for all specifications $T_A = T_J = +25°C$.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55°C	—	+150	°C	
Storage Temperature	T_S	–55°C	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
8-lead DFN	θ_{JA}	—	44	—	°C/W	**Note 1**
8-lead SOIC	θ_{JA}	—	101	—	°C/W	**Note 1**

Note 1: 1 oz., four-layer, 3” x 4” PCB

2.0 PIN DESCRIPTION

Table 2-1 and Table 2-2 show the description of pins in TC6320 8-lead DFN and 8-lead SOIC, respectively. Refer to **Package Types** for the location of pins.

TABLE 2-1: 8-LEAD DFN PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	SN	Source N-channel
2	GN	Gate N-channel
3	GP	Gate P-channel
4	SP	Source P-channel
5	DP	Drain P-channel
6	DP	Drain P-channel
7	DN	Drain N-channel
8	DN	Drain N-channel

TABLE 2-2: 8-LEAD SOIC FUNCTION TABLE

Pin Number	Pin Name	Description
1	SN	Source N-channel
2	GN	Gate N-channel
3	SP	Source P-channel
4	GP	Gate P-channel
5	DP	Drain P-channel
6	DP	Drain P-channel
7	DN	Drain N-channel
8	DN	Drain N-channel

3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 and Figure 3-2 illustrate the switching waveforms and test circuits for TC6320.

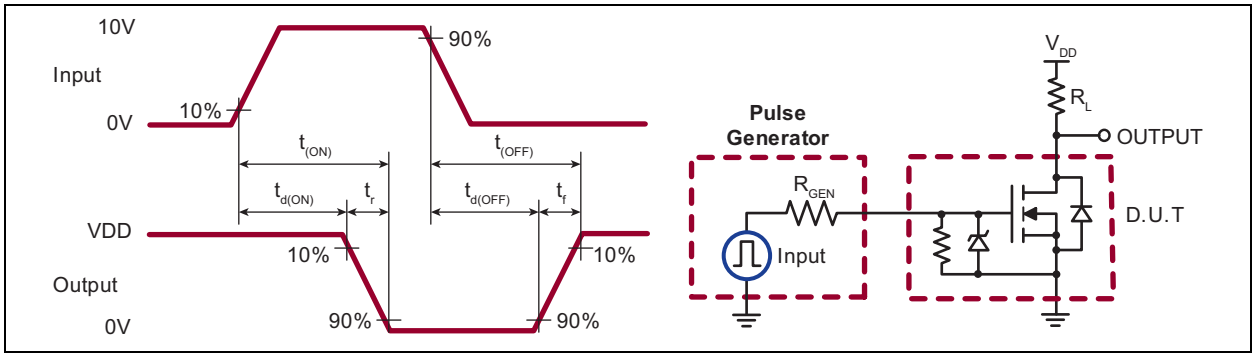


FIGURE 3-1: *N-Channel Switching Waveforms and Test Circuit.*

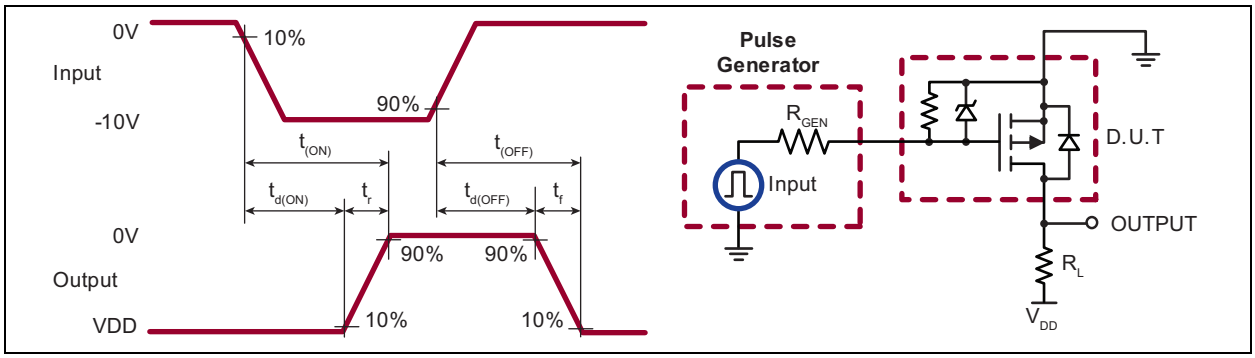


FIGURE 3-2: *P-Channel Switching Waveforms and Test Circuit.*

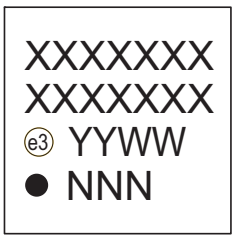
PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)		$R_{DS(ON)}$ (Maximum) (Ω)	
N-Channel	**P-Channel**	**N-Channel**	**P-Channel**
200	–200	7	8

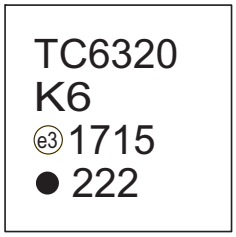
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

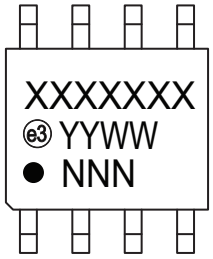
8-lead DFN



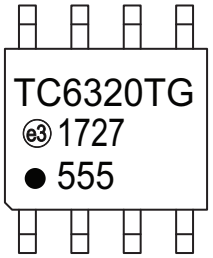
Example



8-lead SOIC



Example

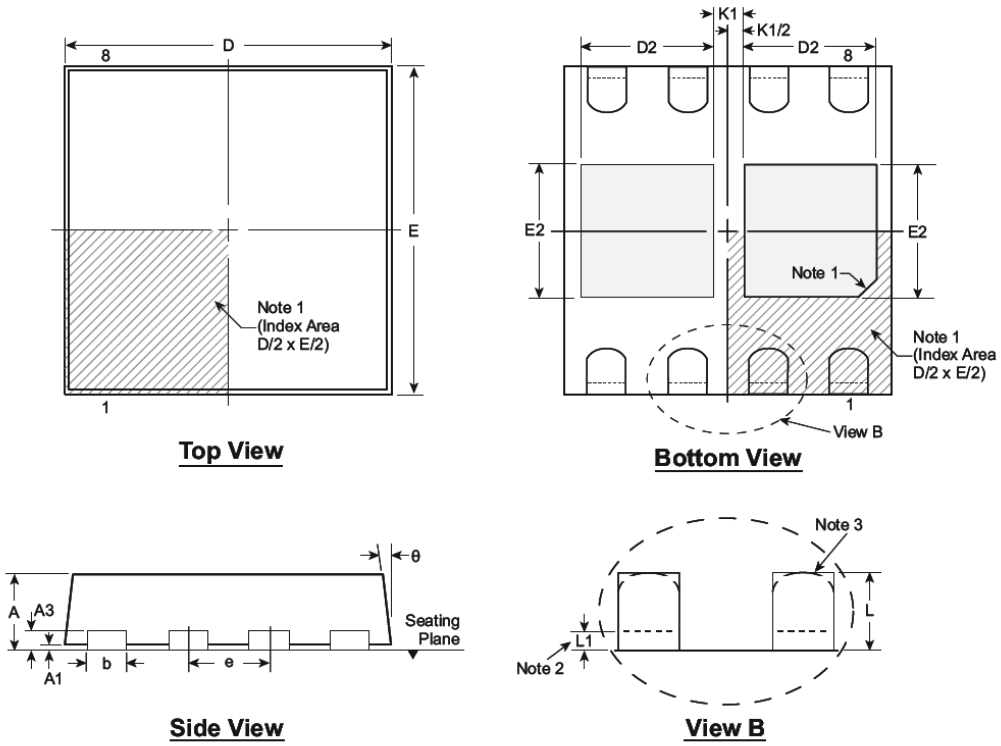


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

8-Lead DFN Package Outline (K6)

4.00x4.00mm body, 1.00mm height (max), 1.00mm pitch (dual pad)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

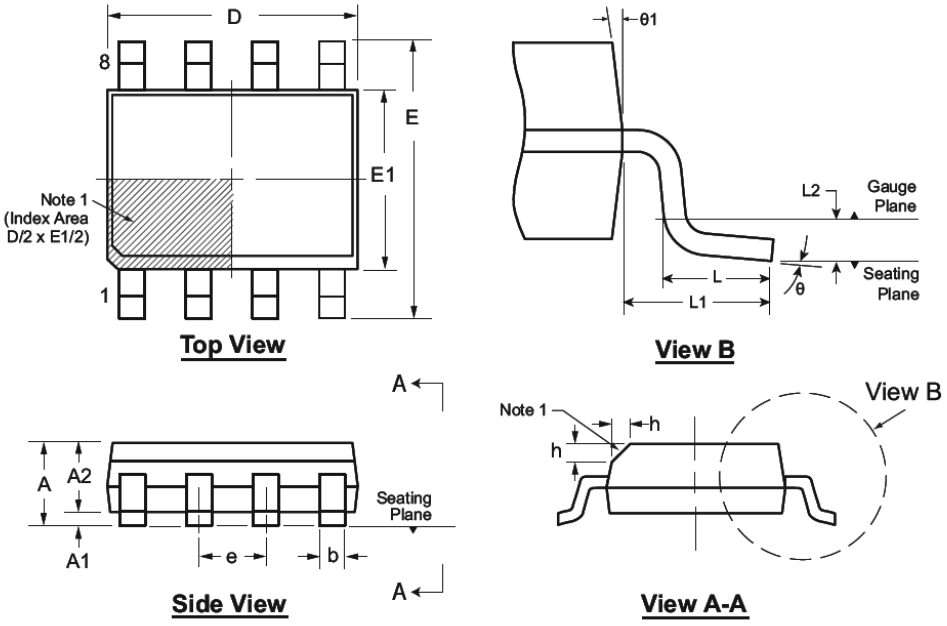
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	K1	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.90	1.35	3.90	1.35	1.00 BSC	0.50 REF	0.40	0.00	0°
	NOM	0.90	-		0.30	4.00	1.45	4.00	1.45			0.50	-	-
	MAX	1.00	0.05		0.35	4.10	1.55	4.10	1.55			0.60	0.15	14°

Drawings not to scale

8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (October 2017)

- Converted Supertex Doc# DSFP-TC6320 to Microchip DS20005697A
- Changed the package marking format
- Changed the quantity of the 8-lead DFN K6 package from 3000/Reel to 3300/Reel
- Changed the quantity of the 8-lead SOIC TG package from 2000/Reel to 3300/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	TC6320	=	N-Channel and P-Channel Enhancement-Mode MOSFET Pair
Packages:	K6	=	8-lead (4x4) VDFN
	TG	=	8-lead SOIC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3300/Reel for a K6 Package
		=	3300/Reel for a TG Package

Examples:

a) TC6320K6-G: N-Channel and P-Channel Enhancement-Mode MOSFET Pair, 8-lead (4x4) VDFN, 3300/Reel

b) TC6320TG-G: N-Channel and P-Channel Enhancement-Mode MOSFET Pair, 8-lead SOIC, 3300/Reel

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