

High-Speed CAN Transceiver with Standby Mode for the Japanese Market – CAN FD Ready

Features

- Compliant with Japanese OEM Requirements
- Certified According to Latest VeLIO (Vehicle LAN Interoperability and Optimization) Test Specification
- Fully ISO 11898-2, ISO 11898-5, ISO 11898-2: 2016 and SAE J2962-2 Compliant
- Communication Speed up to 2 Mbit/s
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- Differential Receiver with Wide Common-Mode Range
- Remote Wake-up Capability via CAN Bus – Wake-up on Pattern (WUP) as Specified in ISO 11898-2: 2016, 3.8 μ s Activity Filter Time
- Functional Behavior Predictable under All Supply Conditions
- Transceiver Disengages from the Bus when Not Powered Up
- RXD Recessive Clamping Detection
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Bus Pins Protected Against Transients in Automotive Environments
- Transmit Data (TXD) Dominant Time-out Function
- Undervoltage Detection on VCC and VIO Pins
- CANH/CANL Short-Circuit and Overtemperature Protected
- Fulfills the OEM “*Hardware Requirements for LIN, CAN and FlexRay™ Interfaces in Automotive Applications*”, Rev. 1.3
- Qualified According to AEC-Q100
- Two Ambient Temperature Grades:
 - ATA6566-GAQW1 and ATA6566-GBQW1 up to $T_{amb} = +125^{\circ}\text{C}$
 - ATA6566-GAQW0 and ATA6566-GBQW0 up to $T_{amb} = +150^{\circ}\text{C}$
- Packages: 8-Pin SOIC, 8-Pin VDFN with Wettable Flanks (Moisture Sensitivity Level 1)

Applications

Classical CAN and CAN FD networks in Automotive, Industrial, Aerospace, Medical and Consumer applications.

General Description

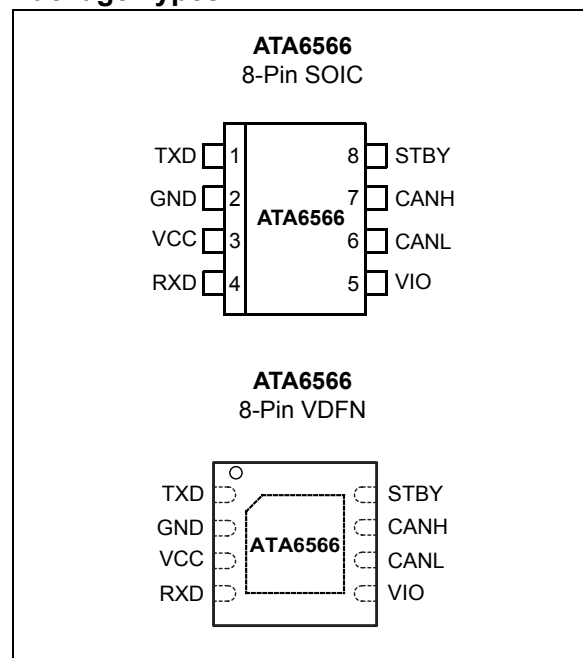
The ATA6566 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed (up to 2 Mbit/s) CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

It offers improved Electromagnetic Compatibility (EMC) and Electrostatic Discharge (ESD) performance, as well as features such as:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- Direct interfacing to microcontrollers with supply voltages from 3V to 5V

Two operating modes, together with the dedicated fail-safe features, make the ATA6566 an excellent choice for all types of high-speed CAN networks, especially in nodes requiring Low-Power mode with wake-up capability via the CAN bus.

Package Types

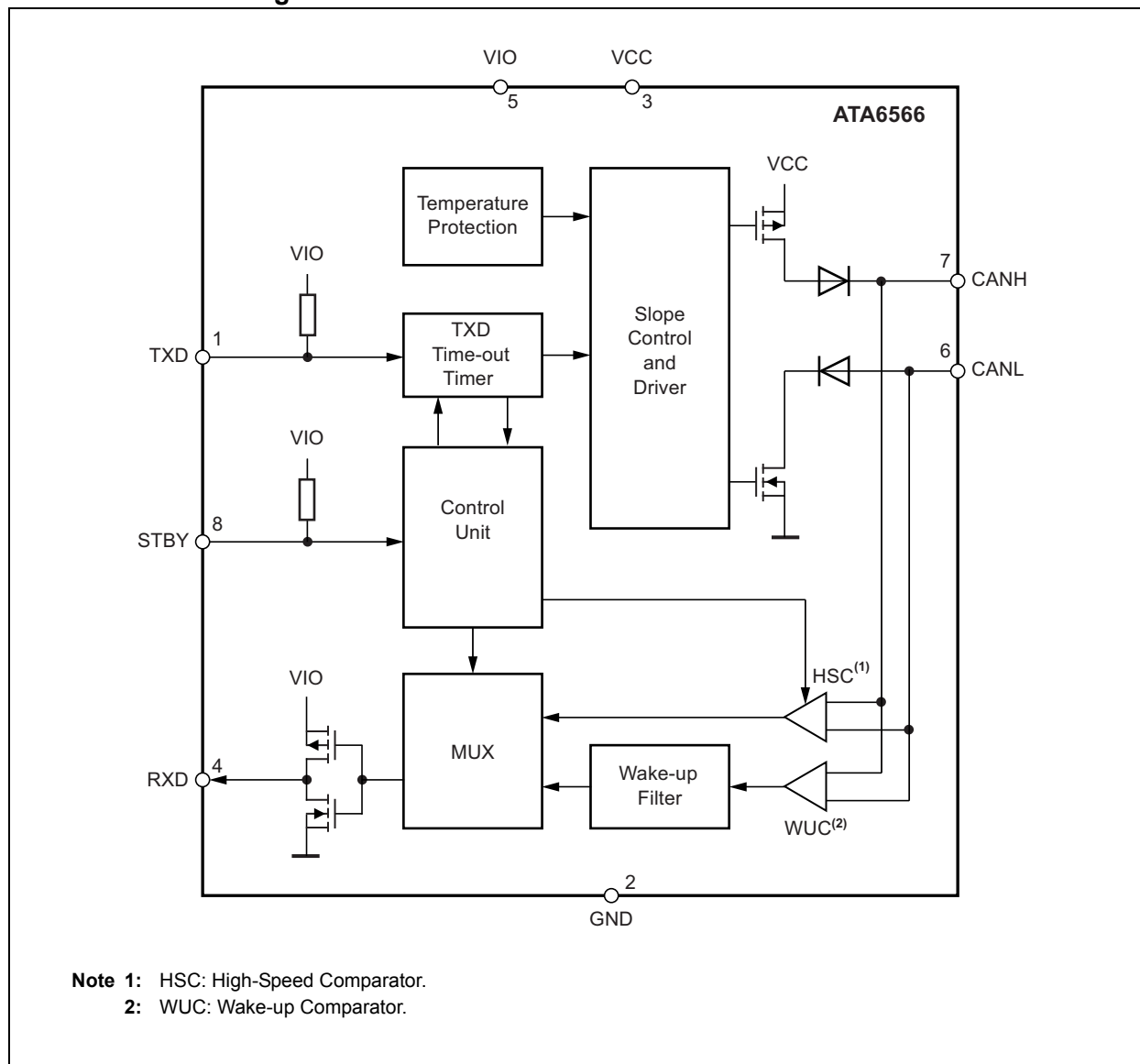


ATA6566

ATA6566 Family Members

Device	Grade 0	Grade 1	VDFN8	SOIC8	Description
ATA6566-GAQW0	X			X	Standby mode, VIO – pin for compatibility with 3.3V and 5V microcontroller
ATA6566-GBQW0	X		X		Standby mode, VIO – pin for compatibility with 3.3V and 5V microcontroller
ATA6566-GAQW1		X		X	Standby mode, VIO – pin for compatibility with 3.3V and 5V microcontroller
ATA6566-GBQW1		X	X		Standby mode, VIO – pin for compatibility with 3.3V and 5V microcontroller

Functional Block Diagram



1.0 FUNCTIONAL DESCRIPTION

The ATA6566 is a stand-alone, high-speed CAN transceiver, compliant with the ISO 11898-2, ISO 11898-2: 2016, ISO 11898-5 and SAE J2962-2 CAN standards. It provides a very low current consumption in Standby mode and wake-up capability via the CAN bus. Pin 5 is the VIO pin and should be connected to the microcontroller supply voltage. This allows direct interfacing to microcontrollers with supply voltages down

to 3V, and adjusts the signal levels of the TXD, RXD and STBY pins to the I/O levels of the microcontroller. The I/O ports are supplied by the VIO pin.

1.1 Operating Modes

The ATA6566 supports two operating modes: Silent and Normal. These modes can be selected via the STBY pin. See [Figure 1-1](#) and [Table 1-1](#) for a description of the operating modes.

FIGURE 1-1: OPERATING MODES

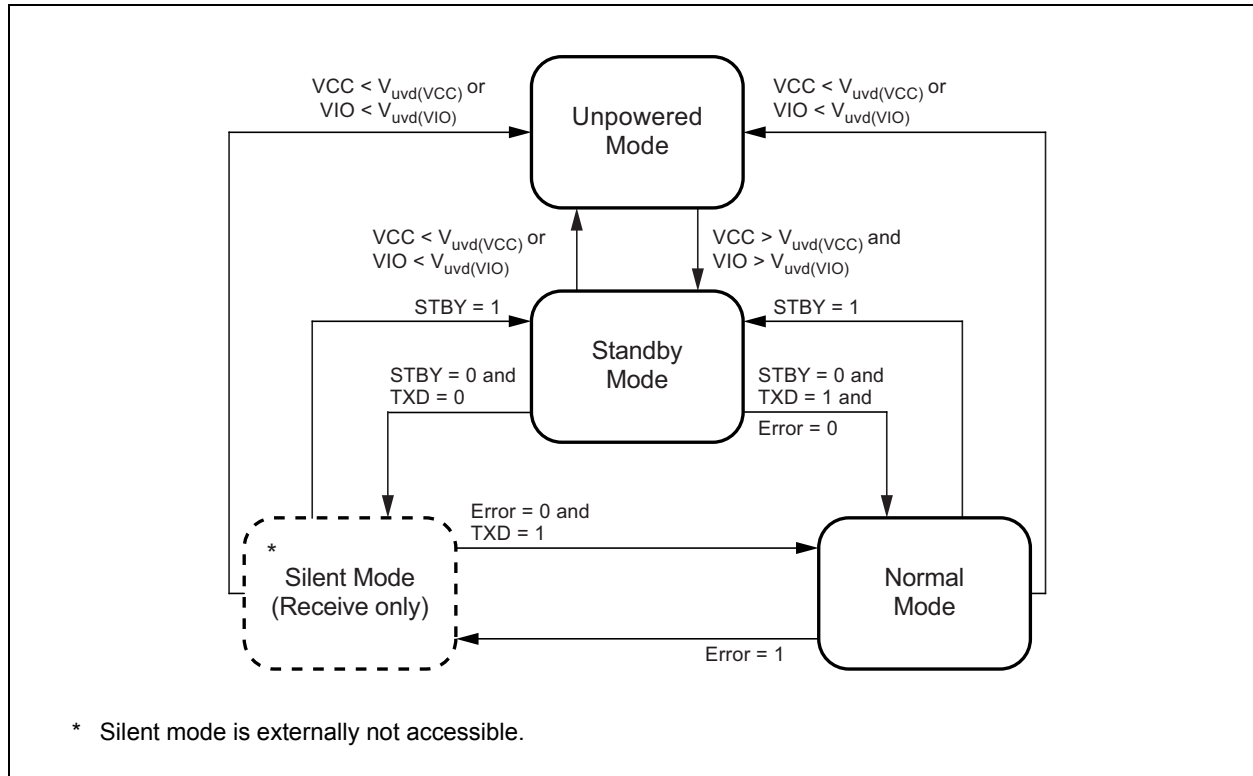


TABLE 1-1: OPERATING MODES

Mode	Inputs		Outputs	
	STBY	Pin TXD	CAN Driver	Pin RXD
Unpowered	X ⁽¹⁾	X ⁽¹⁾	Recessive	Recessive
Standby	High	X ⁽¹⁾	Recessive	Active ⁽²⁾
Normal	Low	Low	Dominant	Low
	Low	High	Recessive	High

Note 1: Irrelevant.

2: Reflects the bus only for wake-up.

ATA6566

1.1.1 NORMAL MODE

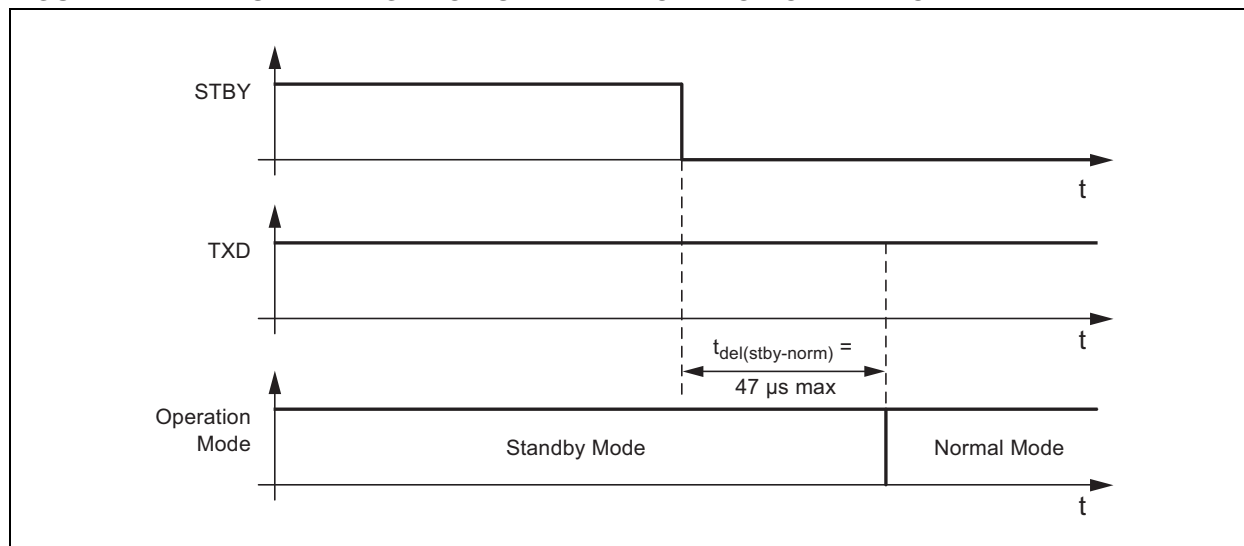
A low level on the STBY pin, together with a high level on the TXD pin, selects the Normal mode. In this mode, the transceiver is able to transmit and receive data via the CANH and CANL bus lines (see the “**Functional Block Diagram**”). The output driver stage is active and drives data from the TXD input to the CAN bus. The High-Speed Comparator (HSC) converts the analog data on the bus lines into digital data, which is output to pin RXD. The bus biasing is set to $V_{VCC}/2$ and the undervoltage monitoring of VCC is active.

The slope of the output signals on the bus lines is controlled and optimized to ensure the lowest possible Electromagnetic Emission (EME).

To switch the device to Normal Operating mode, set the STBY pin to low and the TXD pin to high (see [Table 1-1](#) and [Figure 1-2](#)). The STBY and TXD pins each provide a pull-up resistor to VIO, ensuring defined levels if the pins are open.

Please note that the device cannot enter Normal mode as long as TXD is at ground level.

FIGURE 1-2: SWITCHING FROM STANDBY MODE TO NORMAL MODE



1.1.2 STANDBY MODE

A high level on the STBY pin selects Standby mode. In this mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and the High-Speed Comparator (HSC) are switched off to reduce current consumption.

1.1.3 REMOTE WAKE-UP VIA THE CAN BUS

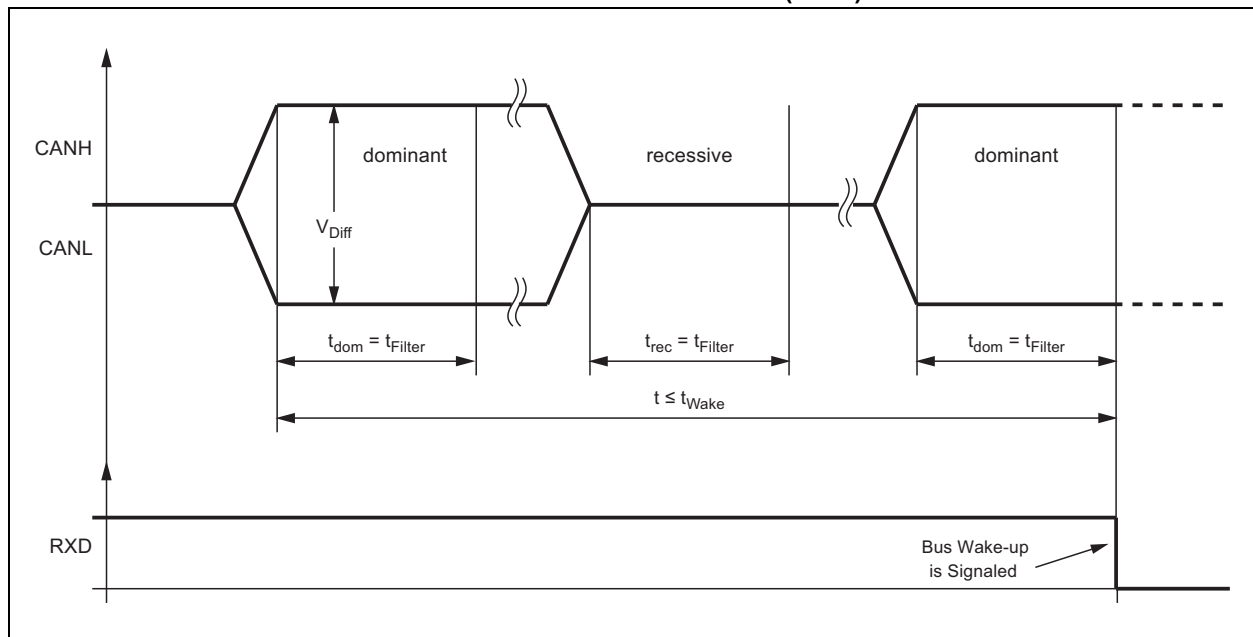
In Standby mode, the bus lines are biased to ground to reduce current consumption to a minimum. The ATA6566 monitors the bus lines for a valid wake-up pattern, as specified in the ISO 11898-2: 2016. This filtering helps to avoid spurious wake-up events that would be triggered by scenarios, such as a dominant clamped bus or by a dominant phase due to noise, spikes on the bus, automotive transients or EMI. The wake-up pattern consists of at least two consecutive dominant bus levels for a duration of at least t_{Filter} , each separated by a recessive bus level with a duration of at

least t_{Filter} . Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern, as shown in Figure 1-3, must be received within the bus wake-up time-out time, t_{Wake} , to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset and then the complete wake-up pattern must be retransmitted to trigger a wake-up event. The RXD pin remains at a high level until a valid wake-up event has been detected.

During normal mode, at a VCC or VIO undervoltage condition or when the complete wake-up pattern is not received within t_{Wake} , no wake-up is signaled at the RXD pin.

When a valid CAN wake-up pattern is detected on the bus, the RXD pin switches to low to signal a wake-up request. A transition to Normal mode is not triggered until the STBY pin is forced back to low by the microcontroller.

FIGURE 1-3: TIMING OF THE BUS WAKE-UP PATTERN (WUP) IN STANDBY MODE



1.2 Fail-Safe Features

1.2.1 TXD DOMINANT TIME-OUT FUNCTION

A TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to a recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high. If the low state on the TXD pin is longer than $t_{to(dom)TXD}$, then the TXD pin has to be set to high $\geq 4 \mu s$ in order to reset the TXD dominant time-out timer.

1.2.2 INTERNAL PULL-UP STRUCTURE AT THE TXD AND STBY INPUT PINS

The TXD and STBY pins have an internal pull-up to VIO. This ensures a safe, defined state in case one or all of these pins are left floating. Pull-up currents flow in these pins in all states, meaning all pins should be in a high state during Standby mode to minimize the current consumption.

1.2.3 UNDERVOLTAGE DETECTION ON PINS VCC AND VIO

If V_{VCC} or V_{VIO} drops below its respective undervoltage detection levels ($V_{uvd(VCC)}$ and $V_{uvd(VIO)}$), see [Section 2.0 "Electrical Characteristics"](#), the transceiver switches off and disengages from the bus until V_{VCC} and V_{VIO} have recovered. The low-power Wake-up Comparator is only

switched off during a VCC or VIO undervoltage. The logic state of the STBY pin is ignored until the VCC voltage or the VIO voltage has recovered.

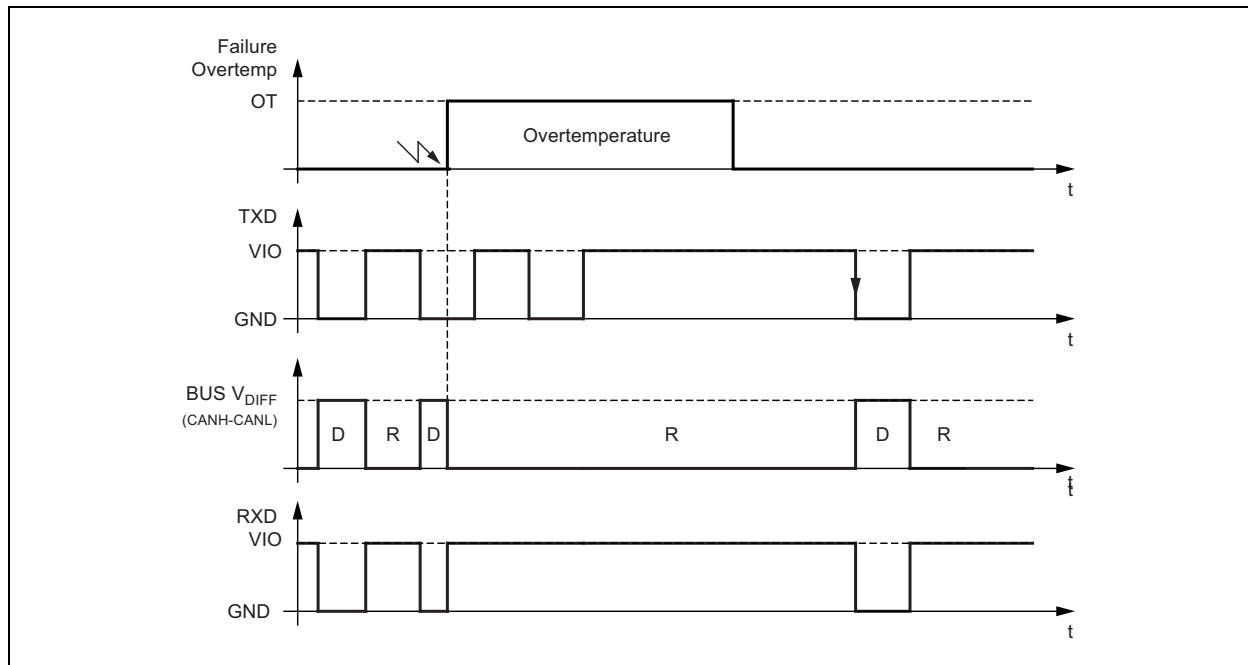
1.2.4 BUS WAKE-UP ONLY AT DEDICATED WAKE-UP PATTERN

Due to the implementation of the wake-up filtering, the ATA6566 does not wake-up when the bus is in a long dominant phase; it only wakes up at a dedicated wake-up pattern as specified in the ISO 11898-2: 2016. This means for a valid wake-up, at least two consecutive dominant bus levels for a duration of at least t_{Filter} , each separated by a recessive bus level with a duration of at least t_{Filter} , must be received via the bus. Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern, as shown in [Figure 1-3](#), must be received within the bus wake-up time-out time, t_{Wake} , to be recognized as a valid wake-up pattern. This filtering leads to a higher robustness against EMI and transients, and therefore, significantly reduces the risk of an unwanted bus wake-up.

1.2.5 OVERTEMPERATURE PROTECTION

The output drivers are protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, T_{Jsd} , the output drivers are disabled until the junction temperature drops below T_{Jsd} and pin TXD is at a high level again. The TXD condition ensures that output driver oscillations due to temperature drift are avoided.

FIGURE 1-4: RELEASE OF TRANSMISSION AFTER OVERTEMPERATURE CONDITION



1.2.6 SHORT-CIRCUIT PROTECTION OF THE BUS PINS

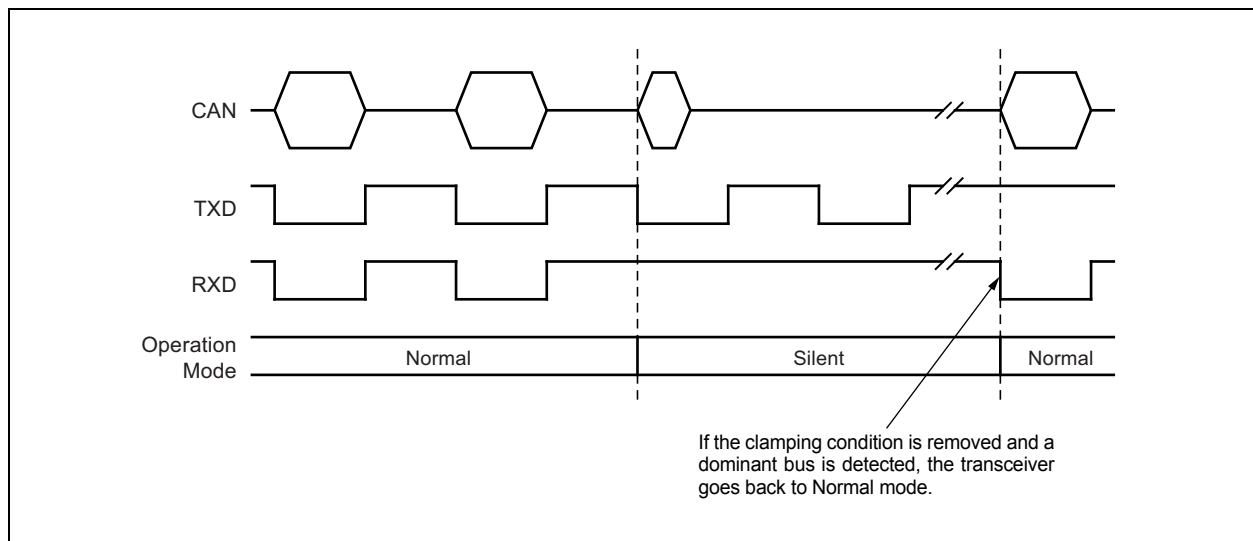
The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage. A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches the bus transmitter off.

1.2.7 RXD RECESSIVE CLAMPING

This fail-safe feature prevents the controller from sending data on the bus if its RXD line is clamped to high (e.g., recessive). That is, if the RXD pin cannot

signalize a dominant bus condition (e.g., because it is shorted to VCC), the transmitter within ATA6566 is disabled to avoid possible data collisions on the bus. In Normal mode, the device permanently compares the state of the High-Speed Comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than t_{RC_det} , without the RXD pin doing the same, a recessive clamping situation is detected and the device is forced into Silent mode (receive only). This Fail-Safe mode is released by either entering Standby or Unpowered mode, or if the RXD pin is showing a dominant (e.g., low) level again.

FIGURE 1-5: RXD RECESSIVE CLAMPING DETECTION



ATA6566

1.3 Pin Descriptions

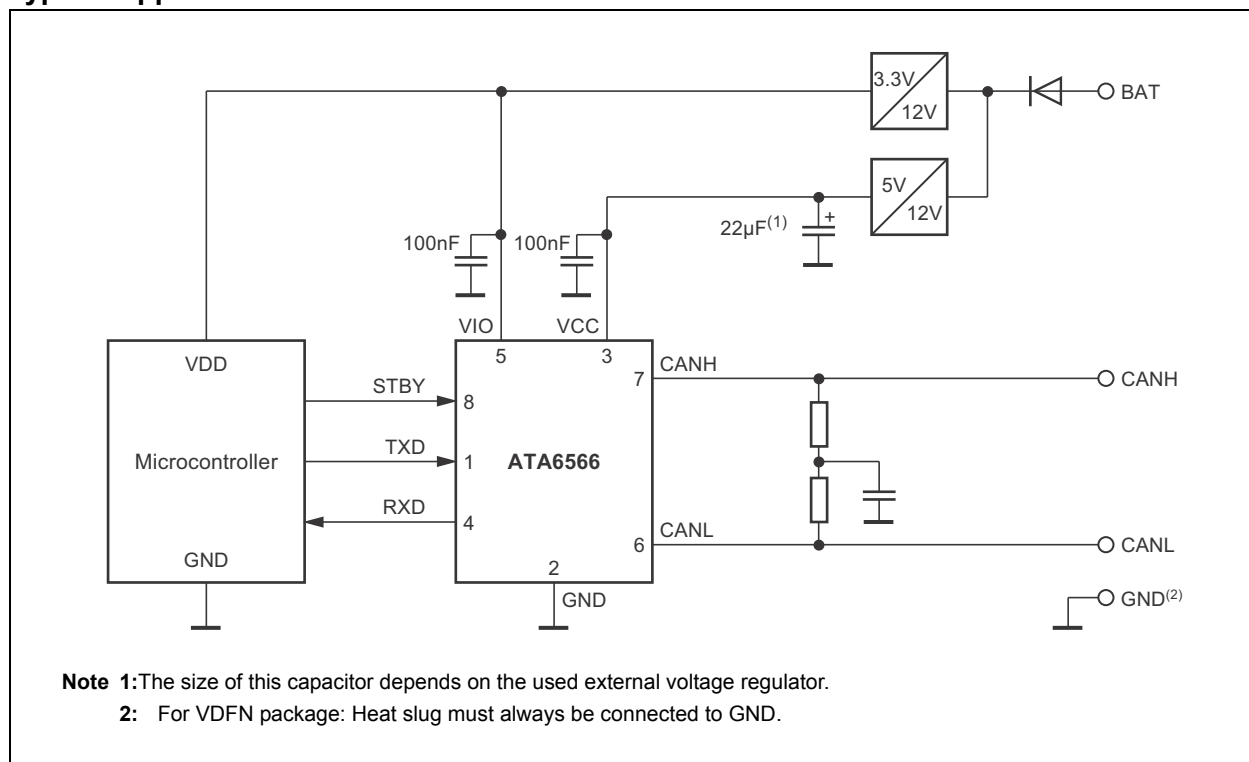
The descriptions of the pins are listed in [Table 1-2](#).

TABLE 1-2: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	TXD	Transmit Data Input
2	GND	Ground Supply
3	VCC	Supply Voltage
4	RXD	Receive Data Output; Reads Out Data from the Bus Lines
5	VIO	Supply Voltage for I/O Level Adapter
6	CANL	Low-Level CAN Bus Line
7	CANH	High-Level CAN Bus Line
8	STBY	Standby Mode Control Input
9	EP ⁽¹⁾	Exposed Thermal Pad: Heat Slug, Internally Connected to the GND Pin

Note 1: Only for the VDFN package.

Typical Application



2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings^(†)

DC Voltage at CANH and CANL	-27V to +42V
Transient Voltage on CANH and CANL (ISO 7637, Part 2)	-150V to +100V
Maximum Differential Bus Voltage	-5V to +18V
DC Voltage on All Other Pins	-0.3V to +5.5V
ESD Protection on CANH and CANL Pins (IEC 61000-4-2)	±8 kV
ESD (HBM following STM 5.1 with 1.5 kΩ/100 pF) – Pins CANH, CANL to GND	±6 kV
Component Level ESD (HBM according to ANSI/ESD STM 5.1), JESD22-A114, AEC-Q 100 (002)	±4 kV
CDM ESD STM 5.3.1	±750V
ESD Machine Model AEC-Q100-RevF(003)	±200V
Virtual Junction Temperature (T_{vj})	-40°C to +175°C
Storage Temperature (T_{stg})	-55°C to +150°C

† Notice: Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ATA6566

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Grade 1: $T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; Grade 0: $T_{amb} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{VCC} = 4.75\text{V}$ to 5.25V ; $V_{VIO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{pF}$ unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply, Pin VCC						
Supply Voltage	V_{VCC}	4.75	—	5.25	V	
Supply Current in Normal Mode	I_{VCC_rec}	2	—	5	mA	Recessive, $V_{TXD} = V_{VIO}$
	I_{VCC_dom}	30	50	70	mA	Dominant, $V_{TXD} = 0\text{V}$
	I_{VCC_short}	—	—	85	mA	Short between CANH and CANL (Note 1)
Supply Current in Standby Mode	I_{VCC_STBY}	—	—	12	μA	$V_{VCC} = V_{VIO}$, $V_{TXD} = V_{VIO}$
	I_{VCC_STBY}	—	7	—	μA	$T_{amb} = +25^{\circ}\text{C}$ (Note 3)
Undervoltage Detection Threshold on Pin VCC	$V_{uvd(VCC)}$	2.75	—	4.5	V	
I/O Level Adapter Supply, Pin VIO						
Supply Voltage on Pin VIO	V_{VIO}	2.8	—	5.5	V	
Supply Current on Pin VIO	I_{VIO_rec}	10	80	250	μA	Normal mode recessive, $V_{TXD} = V_{VIO}$
	I_{VIO_dom}	50	350	500	μA	Normal mode dominant, $V_{TXD} = 0\text{V}$
	I_{VIO_STBY}	—	—	1	μA	Standby mode
Undervoltage Detection Threshold on Pin VIO	$V_{uvd(VIO)}$	1.3	—	2.7	V	
Mode Control Input, Pin STBY						
High-Level Input Voltage	V_{IH}	$0.7 \times V_{VIO}$	—	$V_{VIO} + 0.3$	V	
Low-Level Input Voltage	V_{IL}	-0.3	—	$0.3 \times V_{VIO}$	V	
Pull-up Resistor to VIO	R_{pu}	75	125	175	$\text{k}\Omega$	$V_{STBY} = 0\text{V}$
Low-Level Leakage Current	I_L	-2	—	+2	μA	$V_{STBY} = V_{VIO}$
CAN Transmit Data Input, Pin TXD						
High-Level Input Voltage	V_{IH}	$0.7 \times V_{VIO}$	—	$V_{VIO} + 0.3$	V	
Low-Level Input Voltage	V_{IL}	-0.3	—	$0.3 \times V_{VIO}$	V	
Pull-up Resistor to VIO	R_{TXD}	20	35	50	$\text{k}\Omega$	$V_{TXD} = 0\text{V}$
High-Level Leakage Current	I_{TDX}	-2	—	+2	μA	Normal mode, $V_{TXD} = V_{VIO}$
Input Capacitance	C_{TXD}	—	5	10	pF	(Note 3)
CAN Receive Data Output, Pin RXD						
High-Level Output Current	I_{OH}	-8	—	-1	mA	Normal mode, $V_{RXD} = V_{VIO} - 0.4\text{V}$, $V_{VIO} = V_{VCC}$
Low-Level Output Current	I_{OL}	2	—	12	mA	Normal mode, $V_{RXD} = 0.4\text{V}$, bus dominant
Bus Lines, Pins CANH and CANL						
Single-Ended Dominant Output Voltage	$V_{O(dom)}$	2.75	3.5	4.5	V	$V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$, $R_L = 50\Omega$ to 65Ω , CANH pin
		0.5	1.5	2.25	V	

- Note 1:** Type B: 100% correlation tested.
Note 2: Type C: Characterized on samples.
Note 3: Type D: Design parameter.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Grade 1: $T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; Grade 0: $T_{amb} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$;
 $V_{VCC} = 4.75\text{V}$ to 5.25V ; $V_{VIO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{pF}$ unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Transmitter Voltage Symmetry	V_{Sym}	0.9	1	1.1	—	$V_{Sym} = (V_{CANH} + V_{CANL})/V_{VCC}$ (Note 3)
Bus Differential Output Voltage	V_{Diff}	1.5	—	3	V	$V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$, $R_L = 45\Omega$ to 65Ω
		1.5	—	3.3	V	$V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$, $R_L = 70\Omega$ (Note 3)
		1.5	—	5	V	$V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$, $R_L = 2240\Omega$ (Note 3)
		-50	—	+50	mV	$V_{VCC} = 4.75\text{V}$ to 5.25V , $V_{TXD} = V_{VIO}$, receive, no load
Recessive Output Voltage	$V_{O(rec)}$	2	$0.5 \times V_{VCC}$	3	V	Normal mode, $V_{TXD} = V_{VIO}$, no load
	$V_{O(rec)}$	-0.1	—	+0.1	V	Standby mode, $V_{TXD} = V_{VIO}$, no load
Differential Receiver Threshold Voltage	$V_{th(RX)dif}$	0.5	0.7	0.9	V	Normal mode, $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$
	$V_{th(RX)dif}$	0.4	0.7	1.1	V	Standby mode, $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$ (Note 1)
Differential Receiver Hysteresis Voltage (HSC)	$V_{hys(RX)dif}$	50	120	200	mV	Normal mode, $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$
Differential Receiver Threshold Voltage at Recessive to Dominant Transition	$V_{th(RX)dif_rec_dom}$	0.7	0.8	0.9	V	Normal mode, $V_{cm(CAN)} = -2\text{V}$ to $+7\text{V}$ (Note 1)
Dominant Output Current	$I_{IO(dom)}$	-75	—	-35	mA	$V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$, $V_{VCC} = 5\text{V}$, CANH pin, $V_{CANH} = -5\text{V}$ CANL pin, $V_{CANL} = +40\text{V}$
		35	—	75	mA	
Recessive Output Current	$I_{IO(rec)}$	-5	—	+5	mA	Normal mode, $V_{TXD} = V_{VIO}$, no load, $V_{CANH} = V_{CANL} = -27\text{V}$ to $+32\text{V}$
Leakage Current	$I_{IO(leak)}$	-5	0	+5	μA	$V_{VCC} = V_{VIO} = 0\text{V}$, $V_{CANH} = V_{CANL} = 5\text{V}$
	$I_{IO(leak)}$	-5	0	+5	μA	$V_{VCC} = V_{VIO}$, connected to GND with $47\text{k}\Omega$, $V_{CANH} = V_{CANL} = 5\text{V}$ (Note 3)
Input Resistance	R_i	9	15	28	$\text{k}\Omega$	$V_{CANH} = V_{CANL} = 4\text{V}$
	R_i	9	15	28	$\text{k}\Omega$	$-2\text{V} \leq V_{CANH} \leq +7\text{V}$, $-2\text{V} \leq V_{CANL} \leq +7\text{V}$ (Note 3)

- Note 1:** Type B: 100% correlation tested.
Note 2: Type C: Characterized on samples.
Note 3: Type D: Design parameter.

ATA6566

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Grade 1: $T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; Grade 0: $T_{amb} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$;
 $V_{VCC} = 4.75\text{V}$ to 5.25V ; $V_{VIO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{pF}$ unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Resistance Deviation	ΔR_i	-1	0	+1	%	Between CANH and CANL, $V_{CANH} = V_{CANL} = 4\text{V}$
	ΔR_i	-1	0	+1	%	$-2\text{V} \leq V_{CANH} \leq +7\text{V}$, $-2\text{V} \leq V_{CANL} \leq +7\text{V}$ (Note 3)
Differential Input Resistance	$R_{i(dif)}$	18	30	56	k Ω	$V_{CANH} = V_{CANL} = 4\text{V}$
	$R_{i(dif)}$	18	30	56	k Ω	$-2\text{V} \leq V_{CANH} \leq +7\text{V}$, $-2\text{V} \leq V_{CANL} \leq +7\text{V}$ (Note 3)
Common-Mode Input Capacitance	$C_{i(cm)}$	—	—	20	pF	(Note 3)
Differential Input Capacitance	$C_{i(dif)}$	—	—	10	pF	(Note 3)
Differential Bus Voltage Range for Recessive State Detection	V_{Diff_rec}	-3	—	+0.5	V	Normal and Silent mode (HSC) (Note 3), $-27\text{V} \leq V_{CANH} \leq +27\text{V}$, $-27\text{V} \leq V_{CANL} \leq +27\text{V}$
		-3	—	+0.4	V	Standby mode (WUC), (Note 3), $-27\text{V} \leq V_{CANH} \leq +27\text{V}$, $-27\text{V} \leq V_{CANL} \leq +27\text{V}$
Differential Bus Voltage Range for Dominant State Detection	V_{Diff_dom}	0.9	—	8	V	Normal and Silent mode (HSC) (Note 3), $-27\text{V} \leq V_{CANH} \leq +27\text{V}$, $-27\text{V} \leq V_{CANL} \leq +27\text{V}$
		1.15	—	8	V	Normal and Silent mode (WUC) (Note 3), $-27\text{V} \leq V_{CANH} \leq +27\text{V}$, $-27\text{V} \leq V_{CANL} \leq +27\text{V}$
Transceiver Timing, Pins CANH, CANL, TXD and RXD (see Figure 2-1 and Figure 2-2)						
Delay Time from TXD to Bus Dominant	$t_{d(TXD-busdom)}$	—	—	140	ns	Normal mode
Delay Time from TXD to Bus Recessive	$t_{d(TXD-busrec)}$	—	—	140	ns	Normal mode
Delay Time from Bus Dominant to RXD	$t_{d(busdom-RXD)}$	—	—	140	ns	Normal mode
Delay Time from Bus Recessive to RXD	$t_{d(busrec-RXD)}$	—	—	140	ns	Normal mode
Propagation Delay from TXD to RXD	$t_{PD(TXD-RXD)}$	—	—	255	ns	Normal mode, $R_L = 60\Omega$, $C_L = 100\text{pF}$ Rising edge at pin TXD Falling edge at pin TXD
		—	—	255	ns	
TXD Dominant Time-out Time	$t_{to(dom)TXD}$	0.8	—	3	ms	$V_{TXD} = 0\text{V}$, Normal mode
Bus Wake-up Time-out Time	t_{Wake}	0.8	—	3	ms	Standby mode

- Note 1:** Type B: 100% correlation tested.
Note 2: Type C: Characterized on samples.
Note 3: Type D: Design parameter.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Grade 1: $T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; Grade 0: $T_{amb} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{VCC} = 4.75\text{V}$ to 5.25V ; $V_{VIO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{ pF}$ unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Min. Dominant/Recessive Bus Wake-up Time	t_{Filter}	0.5	—	3.8	μs	Standby mode
Delay Time for Standby Mode to Normal Mode Transition	$t_{del(stby-norm)}$	—	—	47	μs	Falling edge at pin STBY
Delay Time for Normal Mode to Standby Mode Transition	$t_{del(norm-stby)}$	—	—	5	μs	Rising edge at pin STBY (Note 3)
Debouncing Time for Recessive Clamping State Detection	t_{RC_det}	—	90	—	ns	$V_{(CANH-CANL)} > 900\text{ mV}$, RXD = High (Note 3)
Transceiver Timing for Higher Bit Rates, Pins CANH, CANL, TXD and RXD (see Figure 2-1 and Figure 2-3), External Capacitor on the RXD Pin, $C_{RXD} \leq 20\text{ pF}$						
Recessive Bit Time on Pin RXD	$t_{Bit(RXD)}$	400	—	550	ns	Normal mode, $t_{Bit(TXD)} = 500\text{ ns}$
Recessive Bit Time on the Bus	$t_{Bit(Bus)}$	435	—	530	ns	Normal mode, $t_{Bit(TXD)} = 500\text{ ns}$
Receiver Timing Symmetry	Δt_{Rec}	-65	—	+40	ns	Normal mode, $t_{Bit(TXD)} = 500\text{ ns}$, $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

- Note 1:** Type B: 100% correlation tested.
Note 2: Type C: Characterized on samples.
Note 3: Type D: Design parameter.

ATA6566

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
8-Lead SOIC						
Thermal Resistance Virtual Junction to Ambient	R_{thvJA}	—	145	—	K/W	
Thermal Shutdown of the Bus Drivers for ATA6566-GAQW1 (Grade 1)	T_{Jsd}	150	175	195	°C	
Thermal Shutdown of the Bus Drivers for ATA6566-GAQW0 (Grade 0)	T_{Jsd}	160	175	195	°C	
8-Lead VDFN						
Thermal Resistance Virtual Junction to Heat Slug	R_{thvJC}	—	10	—	K/W	
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is Soldered to PCB according to JEDEC	R_{thvJA}	—	50	—	K/W	
Thermal Shutdown of the Bus Drivers for ATA6566-GBQW1 (Grade 1)	T_{Jsd}	150	175	195	°C	
Thermal Shutdown of the Bus drivers for ATA6566-GBQW0 (Grade 0)	T_{Jsd}	160	175	195	°C	

FIGURE 2-1: TIMING TEST CIRCUIT FOR THE ATA6566 CAN TRANSCEIVER

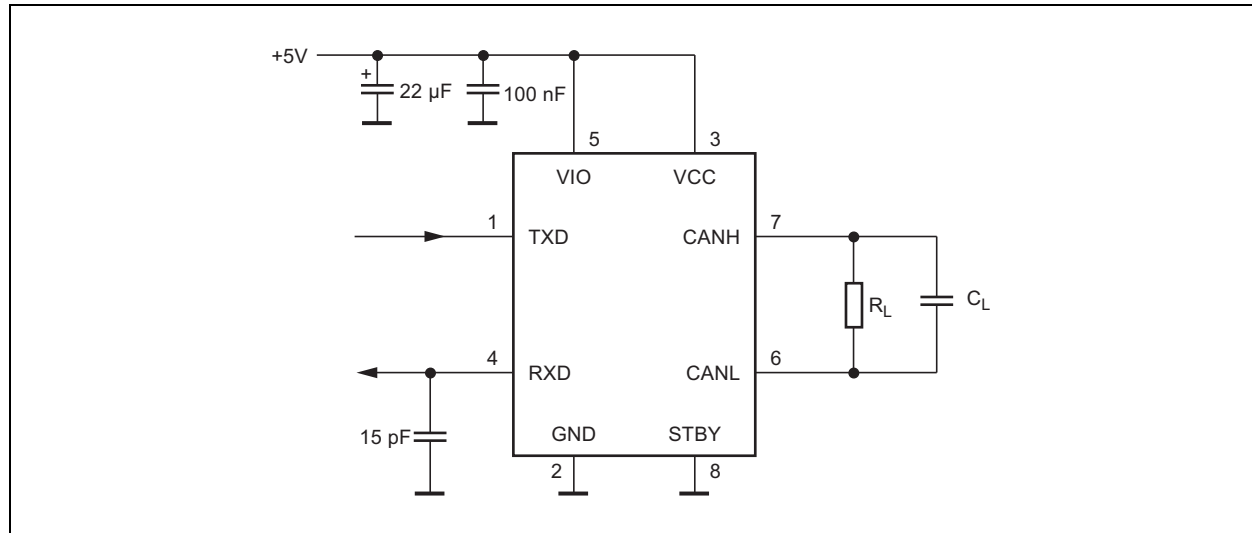


FIGURE 2-2: CAN TRANSCEIVER TIMING DIAGRAM 1

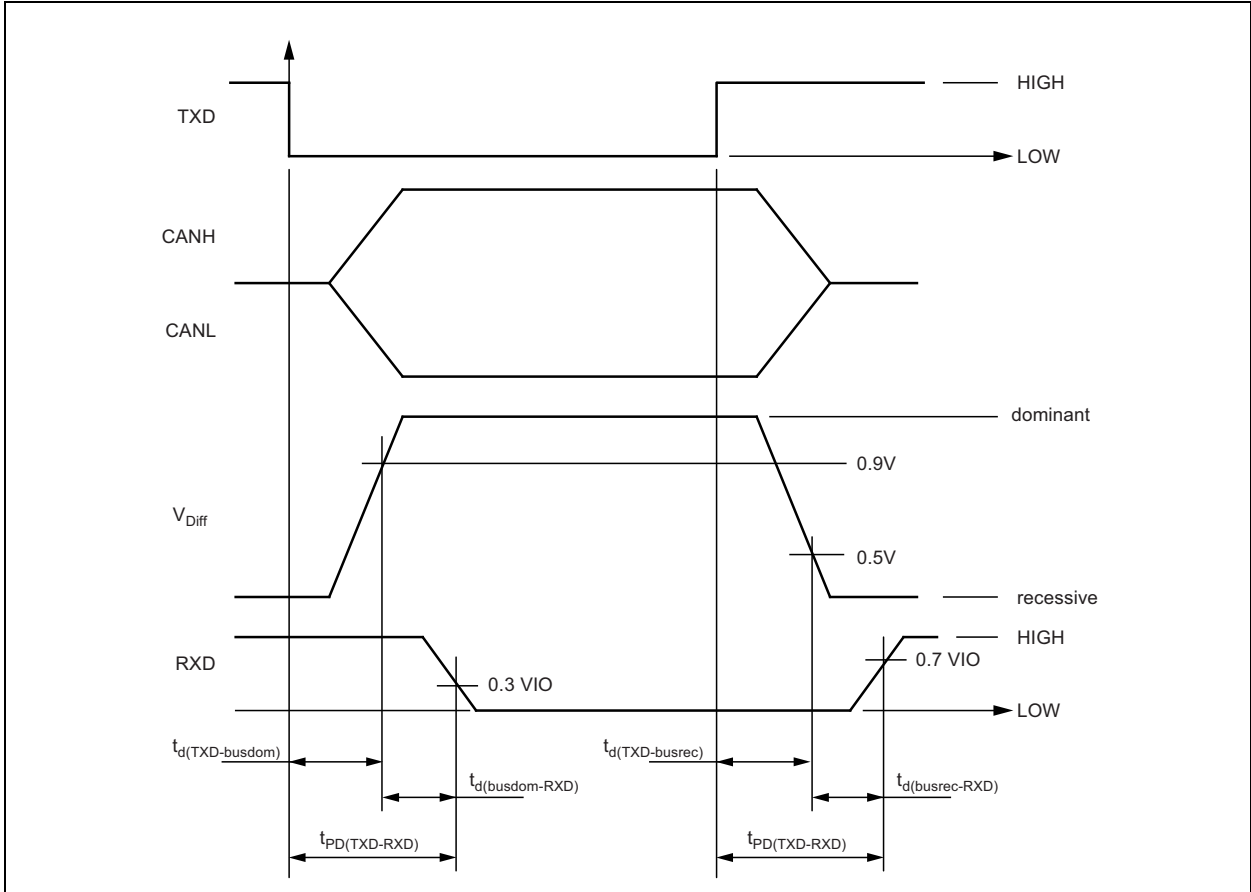
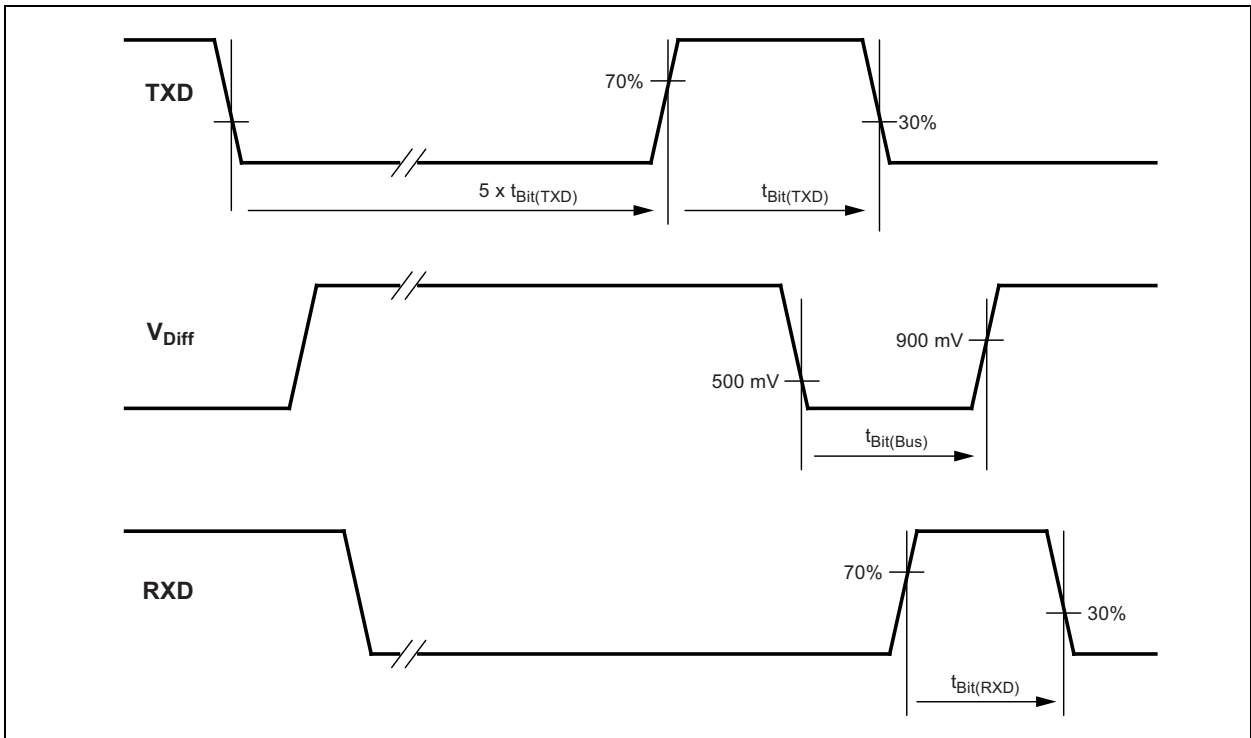


FIGURE 2-3: CAN TRANSCEIVER TIMING DIAGRAM 2

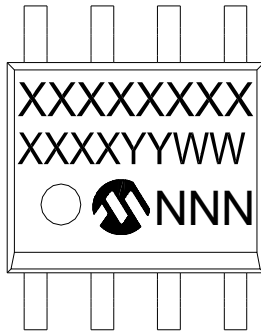


ATA6566

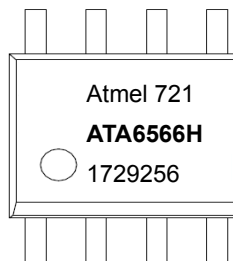
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

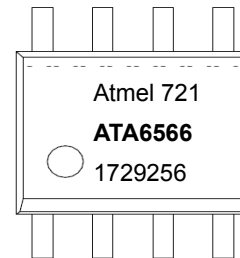
8-Lead SOIC



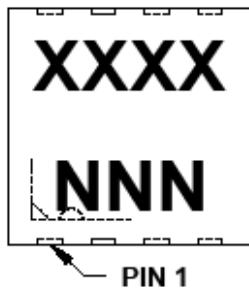
Example, Grade 0



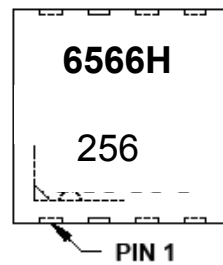
Example, Grade 1



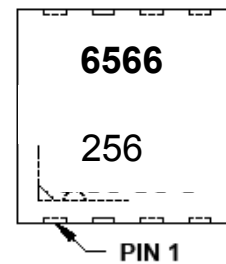
8-Lead 3 x 3 mm VDFN



Example, Grade 0



Example, Grade 1

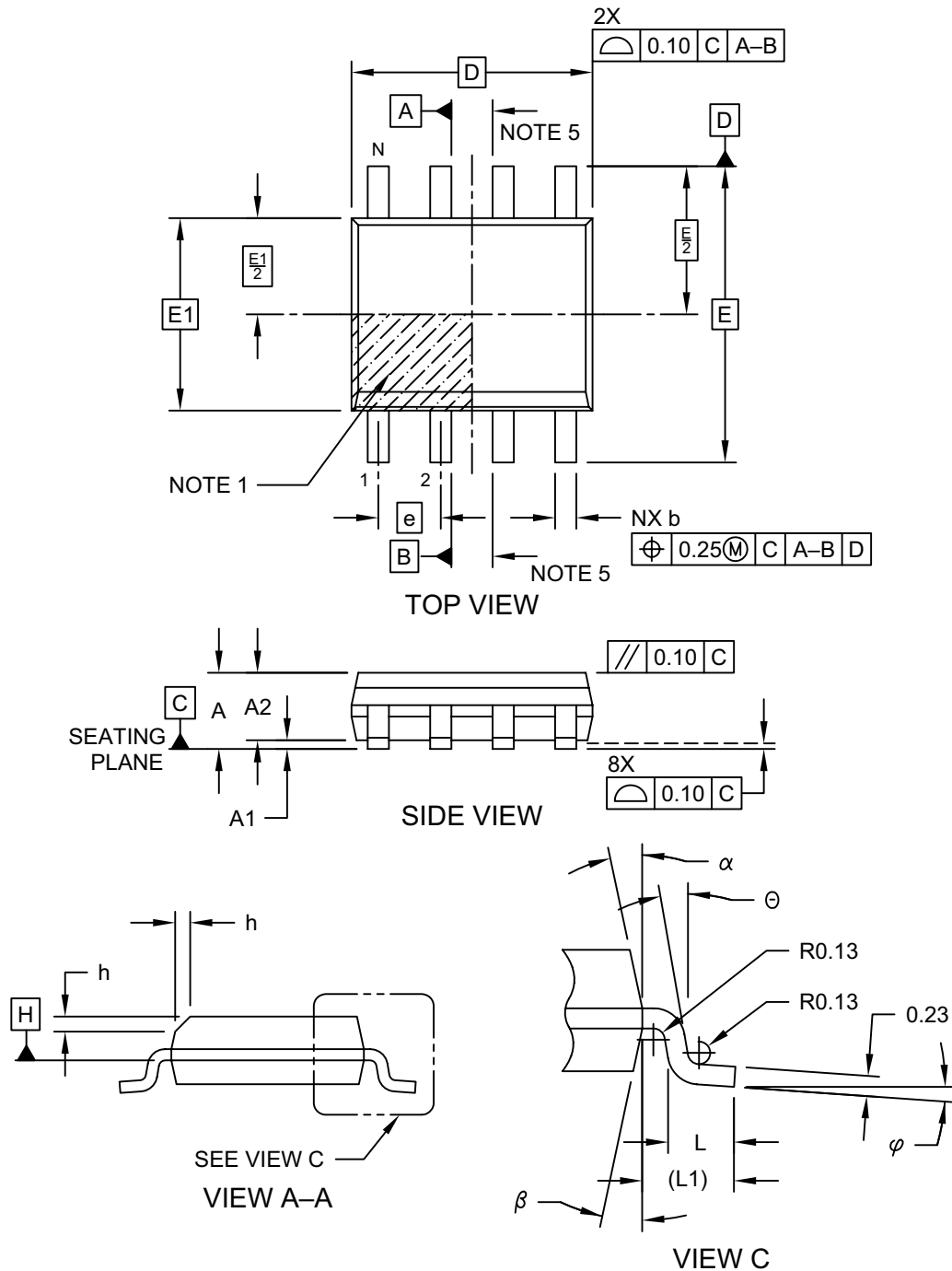


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

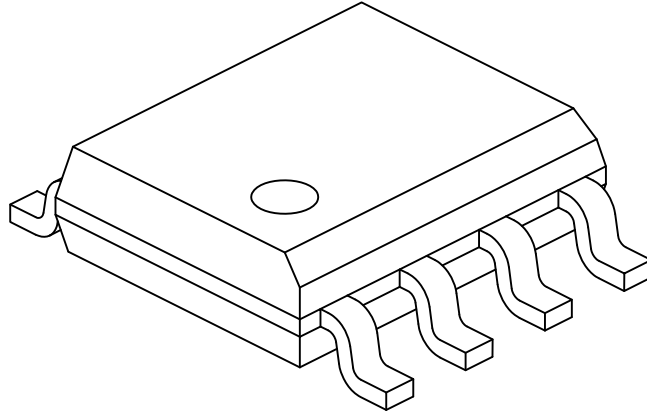


Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

ATA6566

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		1.27 BSC		
Overall Height	A	-	-	-	1.75
Molded Package Thickness	A2		1.25	-	-
Standoff §	A1		0.10	-	0.25
Overall Width	E		6.00 BSC		
Molded Package Width	E1		3.90 BSC		
Overall Length	D		4.90 BSC		
Chamfer (Optional)	h		0.25	-	0.50
Foot Length	L		0.40	-	1.27
Footprint	L1		1.04 REF		
Foot Angle	φ		0°	-	8°
Lead Thickness	c		0.17	-	0.25
Lead Width	b		0.31	-	0.51
Mold Draft Angle Top	α		5°	-	15°
Mold Draft Angle Bottom	β		5°	-	15°

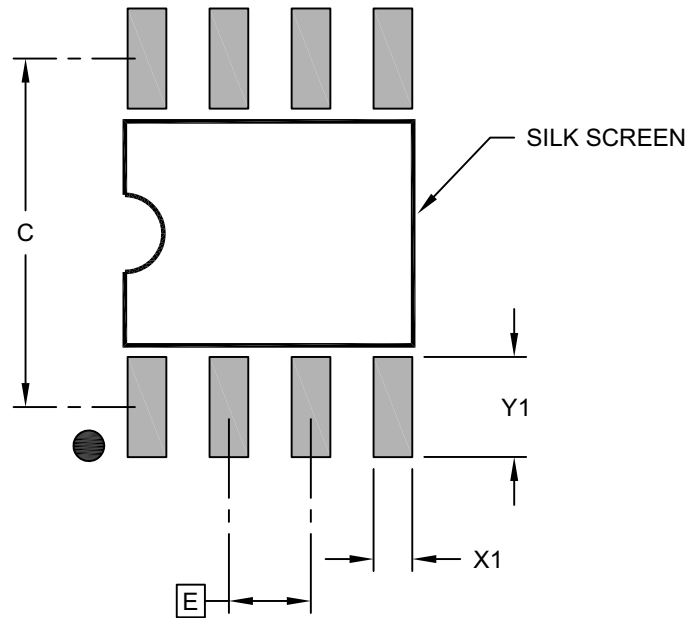
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

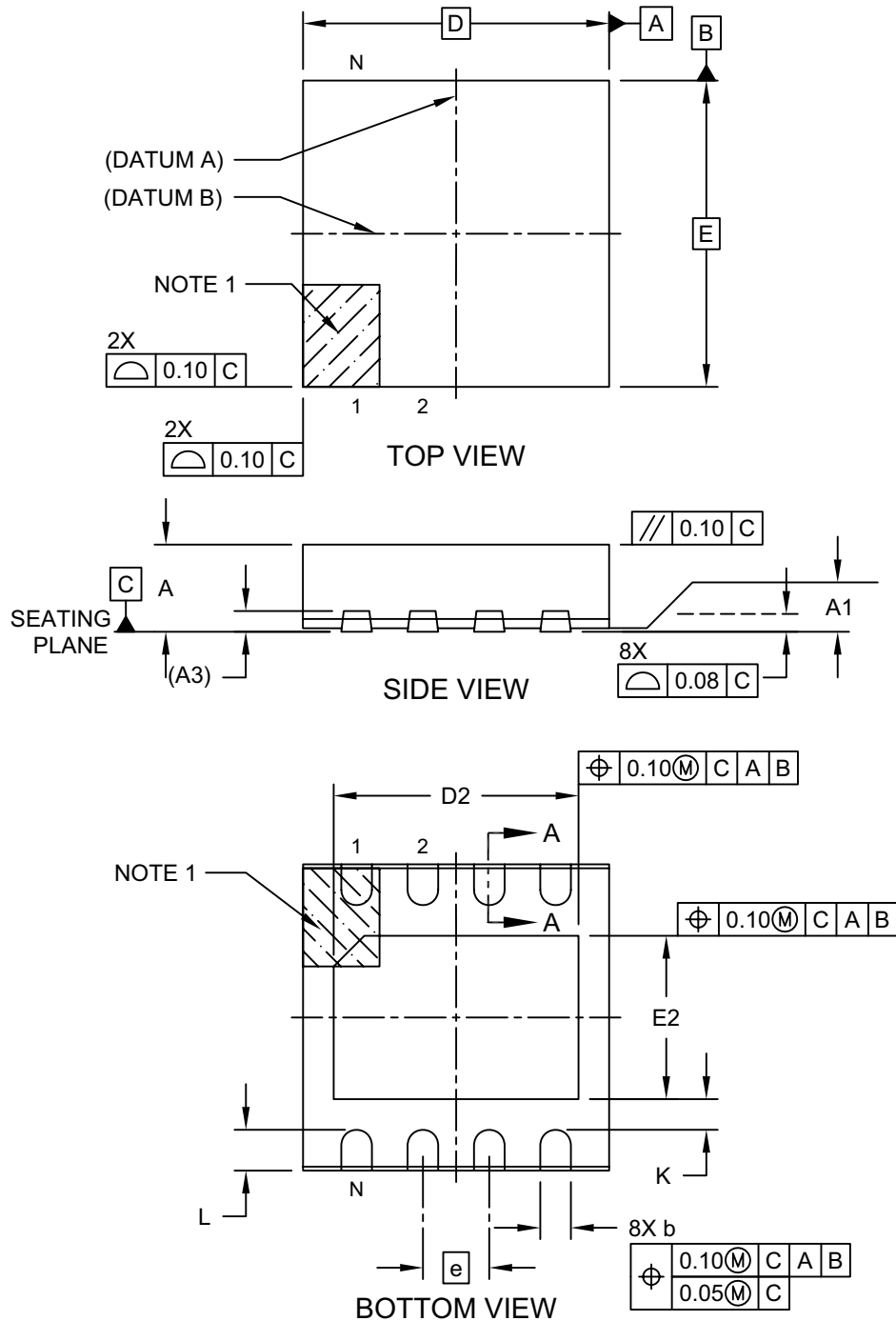
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

ATA6566

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

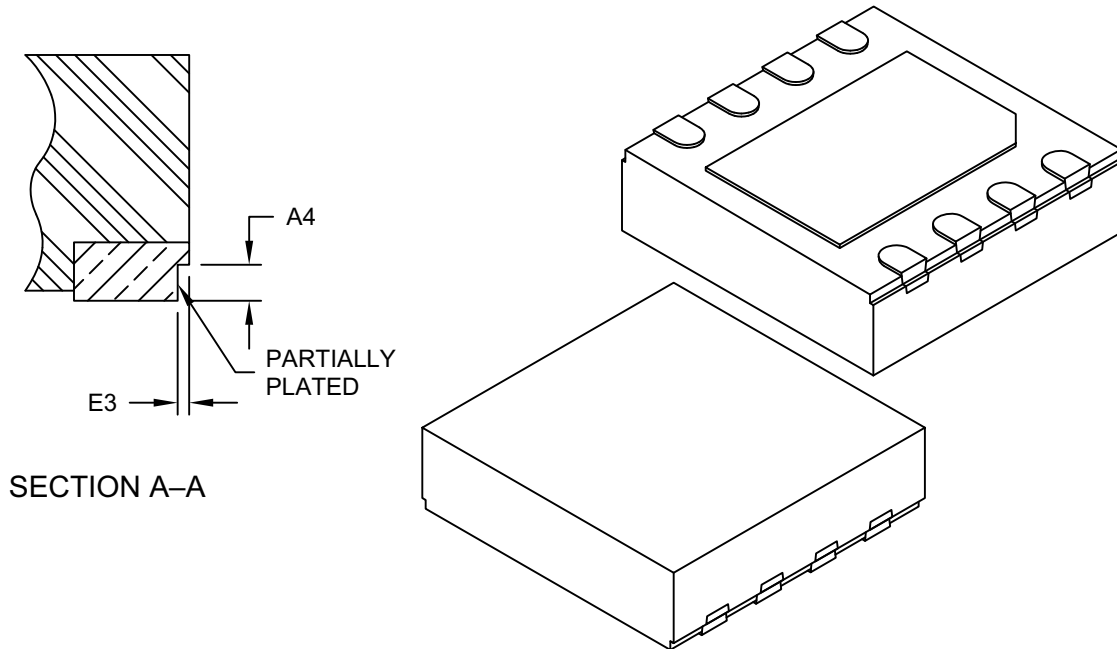
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-21358 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	0.13	0.15
Wettable Flank Step Cut Width	E3	-	-	0.04

Notes:

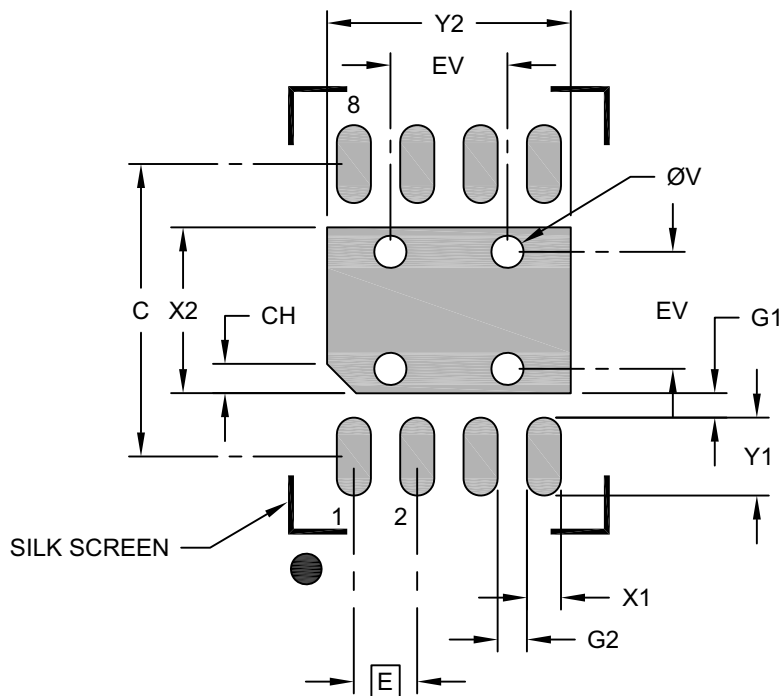
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev B Sheet 2 of 2

ATA6566

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			2.50
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Pin 1 Index Chamfer	CH	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev B

APPENDIX A: REVISION HISTORY

Revision C (September 2017)

The following is the list of modifications:

1. Added the Differential Receiver Threshold Voltage at recessive to Dominant transition parameter in [Section 2.0, Electrical Characteristics](#).
2. Various typographical edits.

Revision B (July 2017)

The following is the list of modifications:

1. Added the new device ATA6566-GBQW0 and updated the related information across the document.
2. Updated [Section “ATA6566 Family Members”](#).
3. Corrected [Section “Electrical Characteristics”](#).
4. Updated [Section “Temperature Specifications”](#).
5. Updated the VDFN8 package drawing and added a Grade 0 package example to [Section 3.1, Package Marking Information](#).
6. Added a ATA6566-GBQW0 example to [Section “Product Identification System”](#).
7. Various typographical edits.

Revision A (June 2017)

- Original Release of this Document.

ATA6566

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	<u>IXI⁽¹⁾</u>	<u>X</u>	<u>X</u>
Device	Package	Tape and Reel Option	Package Directives Classification	Temperature Range
Device:	ATA6566:	High-Speed CAN Transceiver with Standby Mode for the Japanese Market – CAN FD Ready		
Package:	GA =	8-Lead SOIC		
	GB =	8-Lead VDFN		
Tape and Reel Option:	Q =	330 mm diameter Tape and Reel		
Package Directives Classification:	W =	Package according to RoHS ⁽²⁾		
Temperature Range:	0 =	Temperature Grade 0 (-40°C to +150°C)		
	1 =	Temperature Grade 1 (-40°C to +125°C)		

Examples:

a) ATA6566-GAQW0: ATA6566, 8-Lead SOIC, Tape and Reel, Package according to RoHS, Temperature Grade 0

b) ATA6566-GBQW0: ATA6566, 8-Lead VDFN, Tape and Reel, Package according to RoHS, Temperature Grade 0

c) ATA6566-GAQW1: ATA6566, 8-Lead SOIC, Tape and Reel, Package according to RoHS, Temperature Grade 1

d) ATA6566-GBQW1: ATA6566, 8-Lead VDFN, Tape and Reel, Package according to RoHS, Temperature Grade 1

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: RoHS compliant; maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl) and less than 0.15% (1500 ppm) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

ATA6566

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoC® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =**

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KEELoC, KEELoC logo, Klear, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICTail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017, Microchip Technology Incorporated, All Rights Reserved.
ISBN: 978-1-5224-2186-3



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-3326-8000
Fax: 86-21-3326-8021

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

France - Saint Cloud
Tel: 33-1-30-60-70-00

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820