ATA663331/54

LIN System Basis Chip Including LIN Transceiver, Voltage Regulator, Dual Low Side Driver and a High Side Switch

Features

- Supply Voltage up to 40V
- Operating Voltage V_{VS} = 5V to 28V
- Supply Current
  - Sleep Mode: Typically 10 µA
  - Silent Mode: Typically 47 µA
  - Very Low Current Consumption at Low Supply Voltages (2V < V_{VS} < 5.5V): Typically 130 µA
- Linear Low Drop Voltage Regulator, 85 mA Current Capability:
  - MLC (Multi-Layer Ceramic) Capacitor with 0Ω ESR
  - Normal, Fail-Safe and Silent Mode
    ATA663354: V_{VCC} = 5.0V ± 2%
    ATA663331: V_{VCC} = 3.3V ± 2%
  - Sleep Mode: VCC Is Switched Off
- VCC Undervoltage Detection with Open Drain Reset Output (NRES, 4 ms Reset Time)
- Voltage Regulator Is Short Circuit and Overtemperature Protected
- LIN Physical Layer According to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
- Bus Pin Is Overtemperature and Short Circuit Protected versus GND and Battery
- Two Low Side Protected Switches and One High Side Protected Switch
- Wake-Up Capability via LIN Bus (100 µs Dominant) and WKin Pin
- Wake-Up Source Recognition
- TXD Time-Out Timer
- Advanced EMC and ESD Performance
- Fulfills the “OEM Hardware Requirements for LIN in Automotive Applications”, Version.1.3
- Interference and Damage Protection According to ISO7637
- Qualified According to AEC-Q100
- Available in 16-Pin, 3 mm x 5.5 mm VDFN Package with Wettable Flanks (Moisture Sensitivity Level 1)

Applications

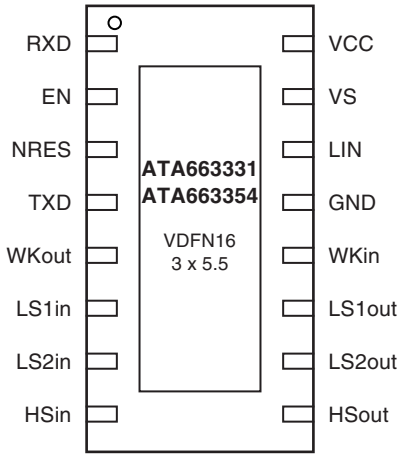
- LIN Networks in Automotive
- Industrial
- Medical
- Consumer Applications

General Description

Designed in compliance with LIN specifications 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2, the ATA6633XX is a new generation of system basis chips with a fully integrated LIN transceiver, a low drop voltage regulator (3.3V/5V/85 mA), two low side drivers, and one high side driver. This combination makes it possible to develop simple, but powerful, slave nodes in LIN bus systems. ATA6633XX is designed to handle low speed data communication in vehicles (such as convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20 kBaud. The bus output is designed to withstand high voltage. Sleep mode and Silent mode guarantee minimized current consumption even in the case of a floating or short circuited LIN bus.

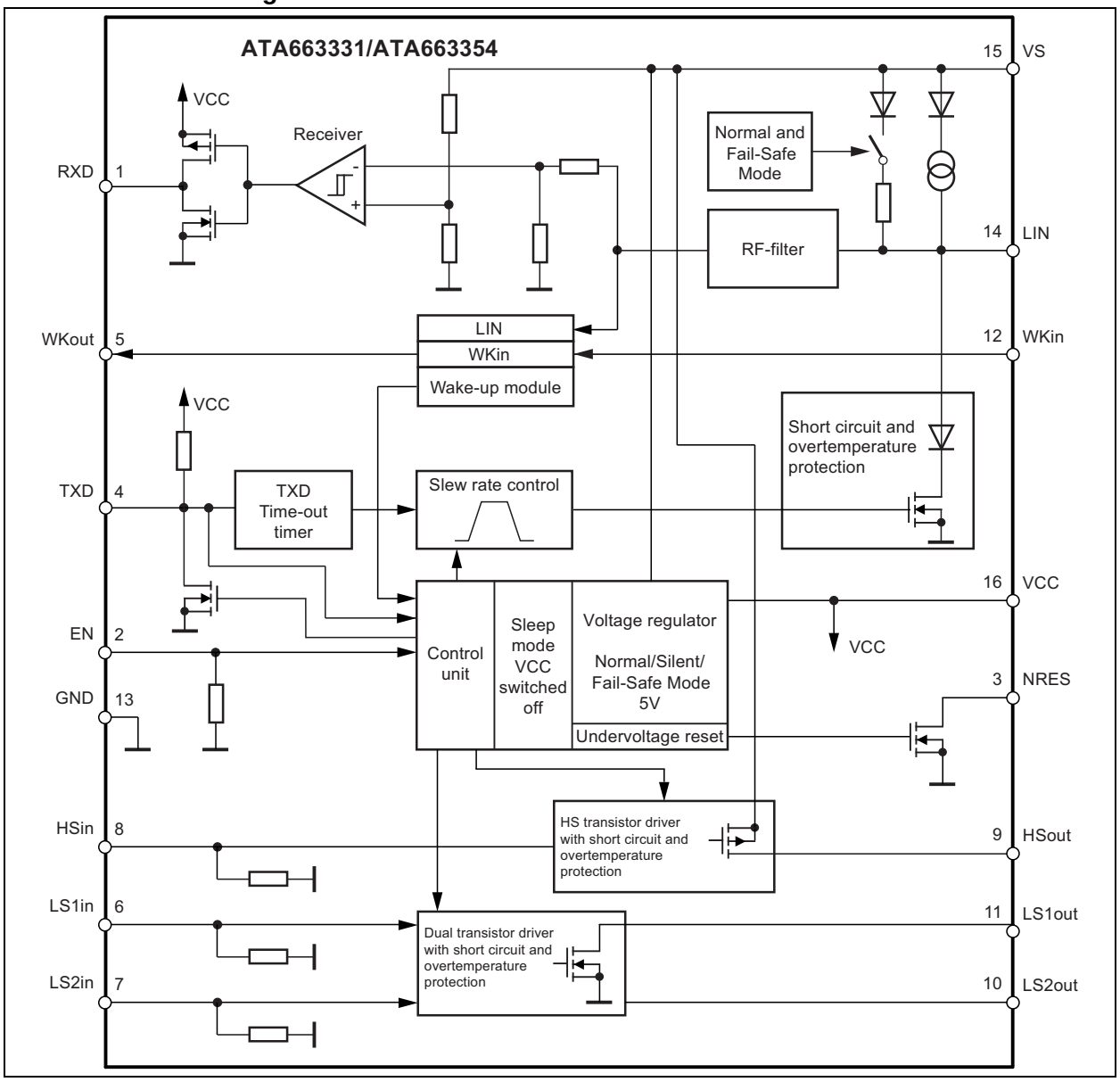
Package Type

ATA663331/54
3 mm x 5.5 mm 16-Lead VDFN*



*Includes Exposed Thermal Pad (EP); see Table 1-4.

Functional Block Diagram



1.0 FUNCTIONAL DESCRIPTION

1.1 Physical Layer Compatibility

Because the LIN physical layer is independent of higher LIN layers (such as the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes found in older versions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

1.2 Operating Modes

FIGURE 1-1: OPERATING MODES

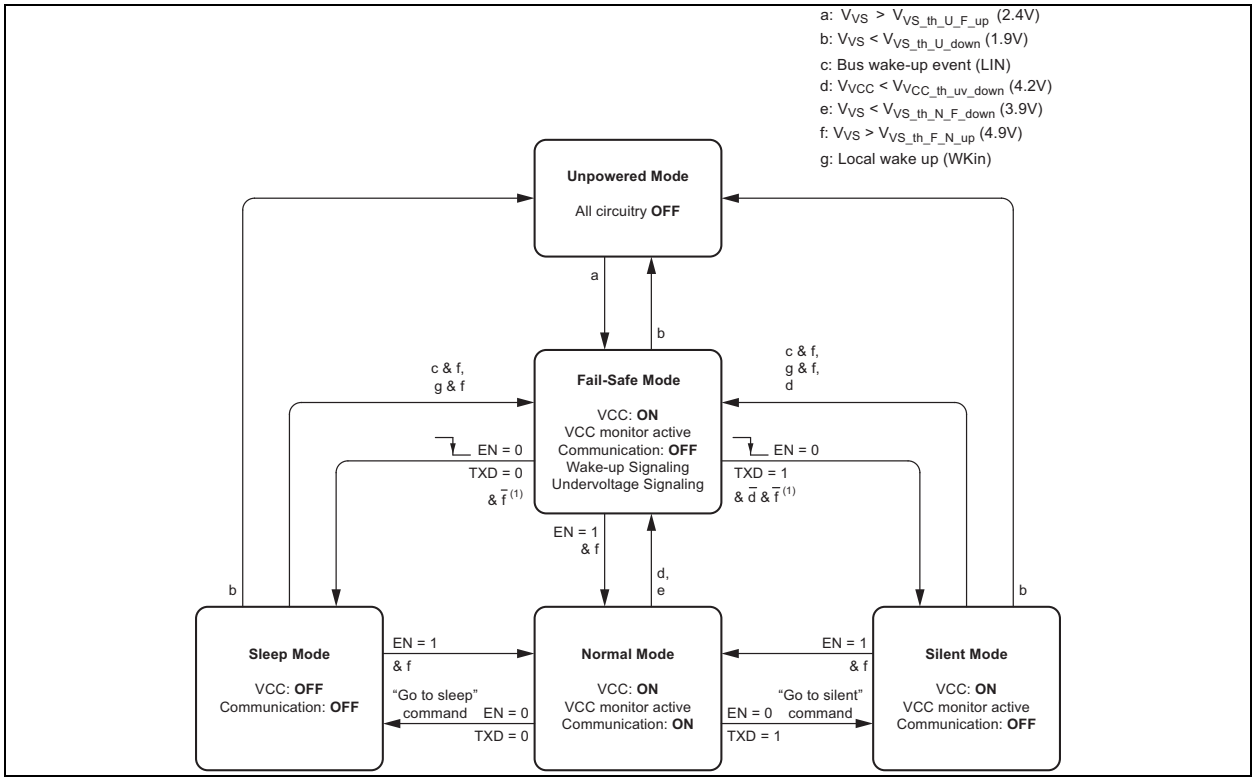


TABLE 1-1: OPERATING MODES

Operating Mode	Transceiver	Voltage Regulator	Low Side Outputs	High Side Output	LIN	TXD	RXD
Fail-Safe	OFF	ON	OFF	HSin-dependent	Recessive	Signaling fail-safe sources (see Table 1-2)	
Normal	ON	ON	LSin-dependent	HSin-dependent	TXD-dependent	Follows data transmission	
Silent	OFF	ON	OFF	HSin-dependent	Recessive	High	High
Sleep/ Unpowered	OFF	OFF	OFF	OFF	Recessive	Low	Low

1.2.1 NORMAL MODE

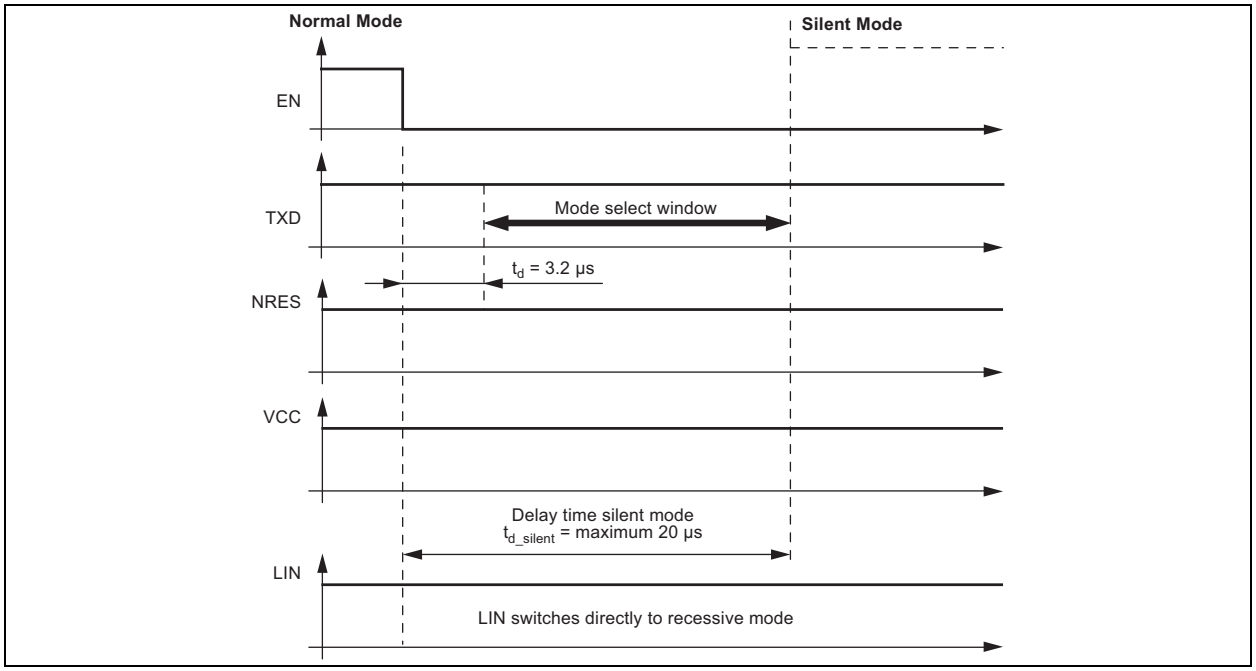
This is the normal transmitting and receiving mode of the LIN Interface. Furthermore, the low side drivers can only be operated in this mode. The VCC voltage regulator works with 3.3V/5V output voltage. If an undervoltage condition occurs, NRES is switched to low and the IC changes its state to Fail-Safe mode.

1.2.2 SILENT MODE

A falling edge at EN while TXD is high switches the IC into Silent mode. The TXD signal has to be logic high during the mode select window. See Figure 1-2.

The transmission path is disabled in Silent mode. The voltage regulator is active. The overall supply current from VBAT is a combination of the $I_{VSsilent}$ of typically 47 µA plus the VCC regulator output current I_{VCC}.

FIGURE 1-2: SWITCHING TO SILENT MODE



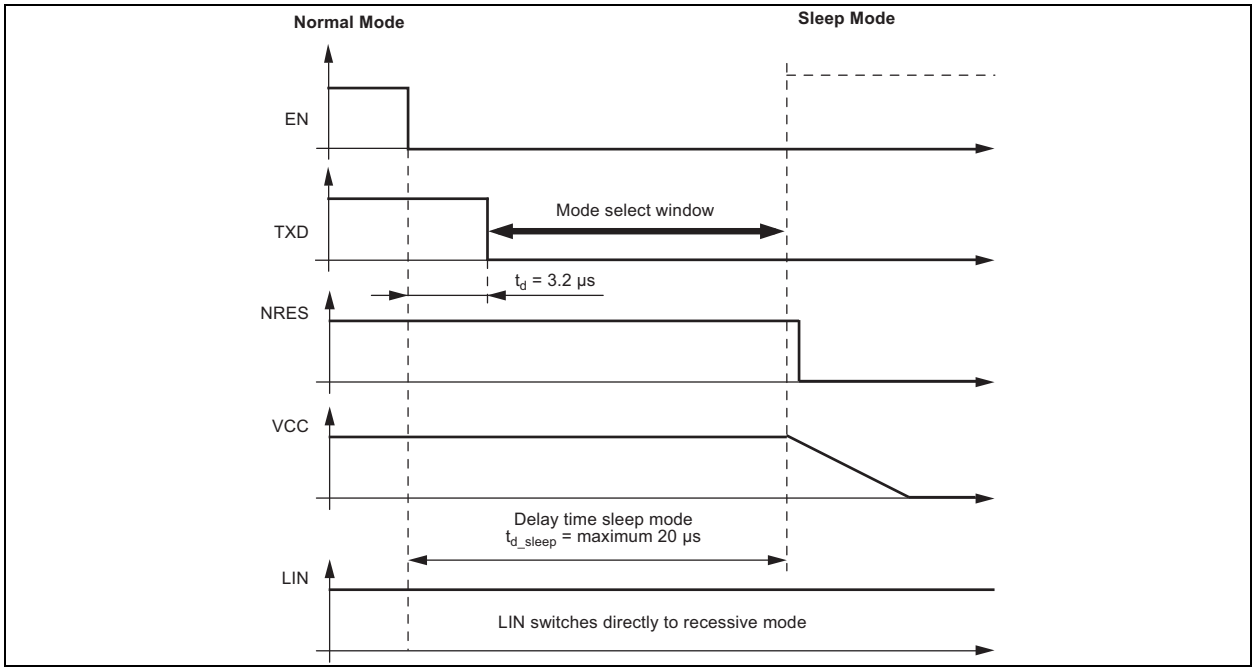
In Silent mode, the internal slave termination between the LIN pin and VS pin is disabled to minimize the current consumption in case the pin LIN is short-circuited to GND. Only a weak pull up current (typically 10 µA) is present between the LIN pin and the VS pin. The Silent mode can be activated regardless of the current level on the LIN pin or WKin pin.

If an undervoltage condition occurs, NRES is switched to low and the ATA6633XX changes its state to Fail-Safe mode.

1.2.3 SLEEP MODE

A falling edge at EN while TXD is low switches the IC into Sleep mode. The TXD signal has to be logic low during the mode select window. See Figure 1-3.

FIGURE 1-3: SWITCHING TO SLEEP MODE



In order to avoid any influence on the LIN pin while switching to Sleep mode, it is possible to switch the EN pin to low up to 3.2 µs earlier than the TXD pin. The best and easiest way is to generate two simultaneous falling edges at TXD and EN.

In Sleep mode, the transmission path is disabled. Supply current from VBAT is typically $I_{VSsleep}$ = 10 µA. The VCC regulator is switched off; NRES and RXD are low. The internal slave termination between pin LIN and pin VS is disabled to minimize the current consumption in case pin LIN is short circuited to GND. Only a weak pull-up current (typically 10 µA) between pin LIN and pin VS is present. Sleep mode can be activated independently from the current level on pin LIN. A voltage less than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer.

If TXD is short circuited to GND, it is possible to switch to Sleep mode via EN after t > t_{dom}.

1.2.4 FAIL-SAFE MODE

The device automatically switches to Fail-Safe mode at system power-up. The voltage regulator is switched on. The NRES output remains low for t_{res} = 4 ms and resets the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to Normal mode. A low at NRES switches the IC directly into Fail-Safe mode. During Fail-Safe mode, the TXD pin is an output and signals the fail-safe source together with the RXD output pin.

If the device enters Fail-Safe mode coming from the Normal mode (EN = 1) due to a V_{VS} undervoltage condition ($V_{VS} < V_{VS\_th\_N\_F\_down}$), it is possible to switch into Sleep or Silent mode through a falling edge at the EN input. The current consumption can be further reduced with this feature.

A wake-up event from either Silent or Sleep mode is signaled to the microcontroller using the RXD pin and the TXD pin. A V_{VS} undervoltage condition is also signaled at these two pins. The coding is shown in Table 1-2.

A wake-up event switches the IC to Fail-Safe mode.

TABLE 1-2: SIGNALING IN FAIL-SAFE MODE

Fail-Safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin)	Low	High
$V_{VS\_th\_N\_F\_down}$ (battery) undervoltage detection (V_{VS} < 3.9V)	High	Low

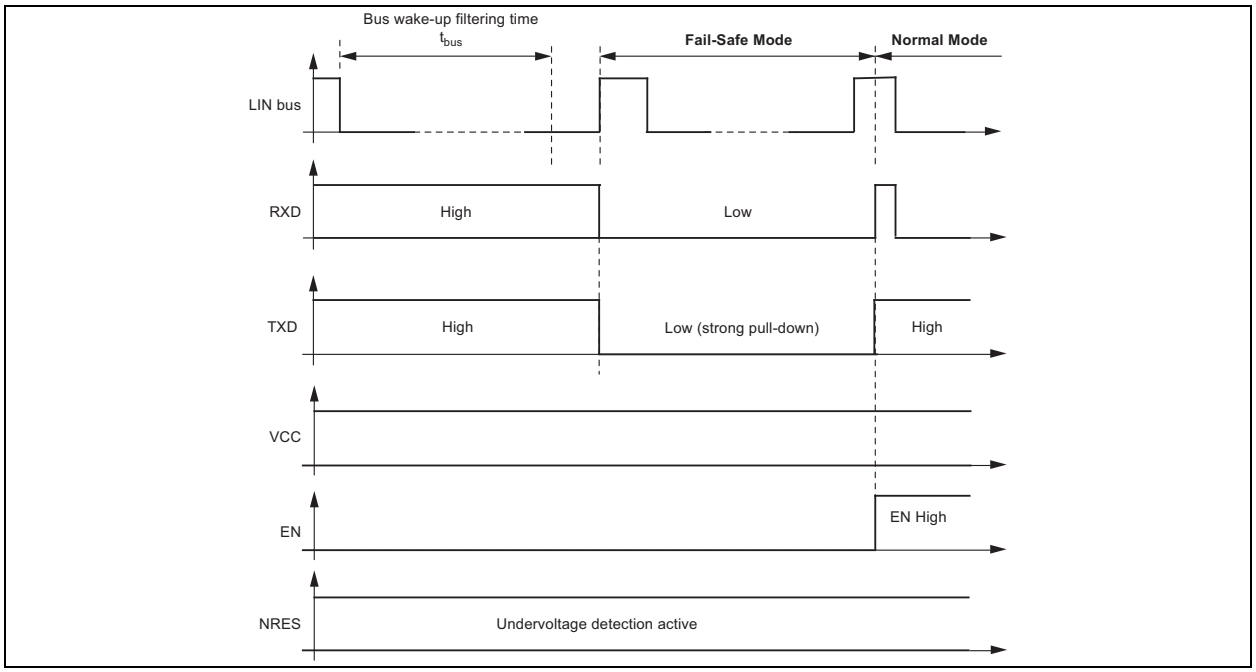
1.3 Wake-Up Scenarios from Silent Mode or Sleep Mode

1.3.1 REMOTE WAKE-UP VIA LIN BUS

1.3.1.1 Remote Wake-up from Silent Mode

A remote wake-up from Silent mode is only possible if TXD is high. A voltage less than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer. A falling edge at the LIN pin followed by a dominant bus level maintained for a certain period of time (> t_{bus}) and the following rising edge at pin LIN (see Figure 1-4) results in a remote wake-up request. The device switches from Silent mode to Fail-Safe mode, the VCC voltage regulator remains activated and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD pin and TXD pin (strong pull down at TXD). EN high can be used to switch directly to Normal mode.

FIGURE 1-4: LIN WAKE-UP FROM SILENT MODE



1.3.1.2 Remote Wake-Up from Sleep Mode

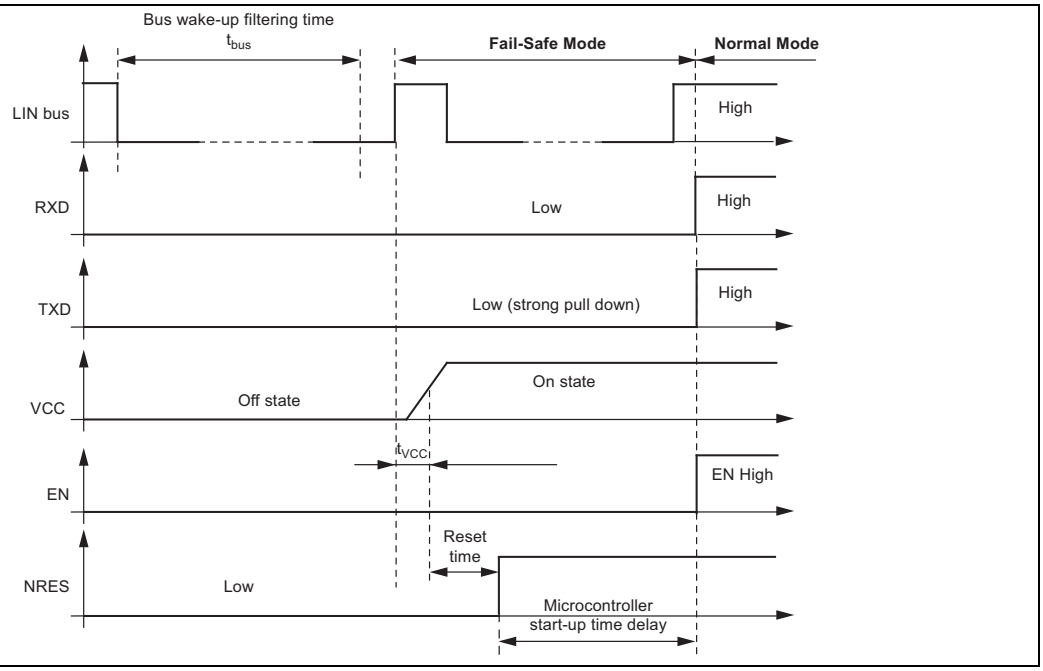
A voltage less than the LIN pre-wake detection V_{LINL} at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain period of time (> t_{bus}) with a subsequent rising edge at the LIN pin results in a remote wake-up request. The device switches from Sleep mode to Fail-Safe mode.

The VCC regulator is activated, and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at RXD and TXD (strong pull down at TXD). See Figure 1-5.

EN high can be used to switch directly from Sleep/Silent mode to Normal mode. If EN is still high after V_{VCC} ramp-up and the undervoltage reset time, the IC switches to Normal mode.

FIGURE 1-5: LIN WAKE-UP FROM SLEEP MODE



1.3.2 LOCAL WAKE-UP VIA WKin PIN

A falling edge at the WKin pin followed by a low level maintained for a given time period (> t_{WKin}) results in a local wake-up request. The device switches to Fail-Safe mode. The internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD pin to generate an interrupt for the microcontroller. When the WKin pin is low, it is possible to switch to Silent mode or Sleep mode via the EN pin. In this case, the wake-up signal has to be switched to high > 10 µs before the negative edge at WKin starts a new local wake-up request.

FIGURE 1-6: LOCAL WAKE-UP FROM SLEEP MODE

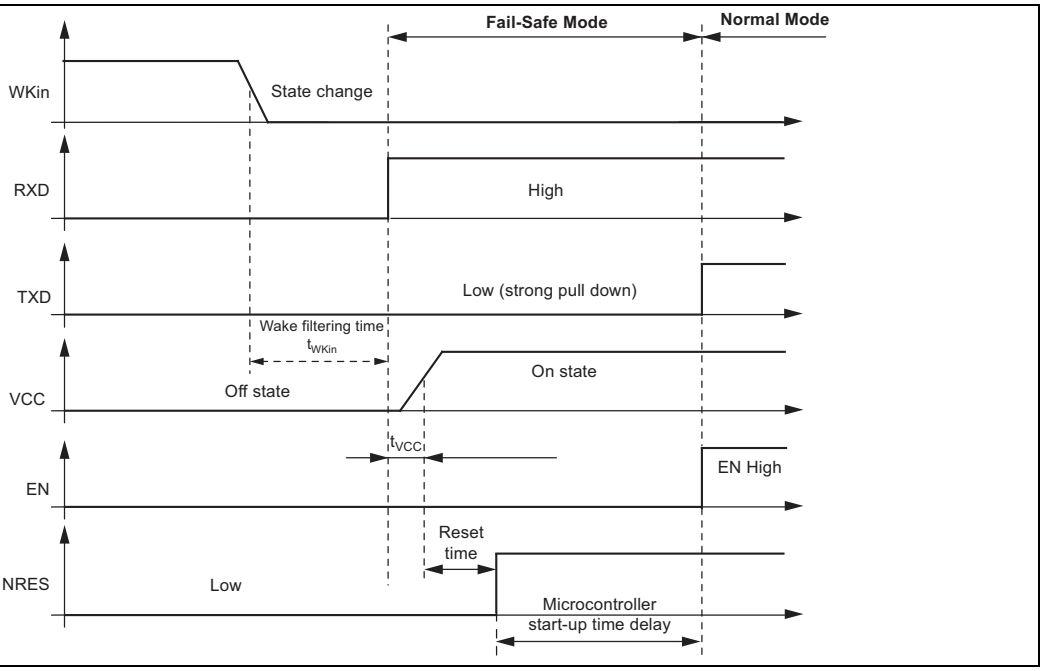
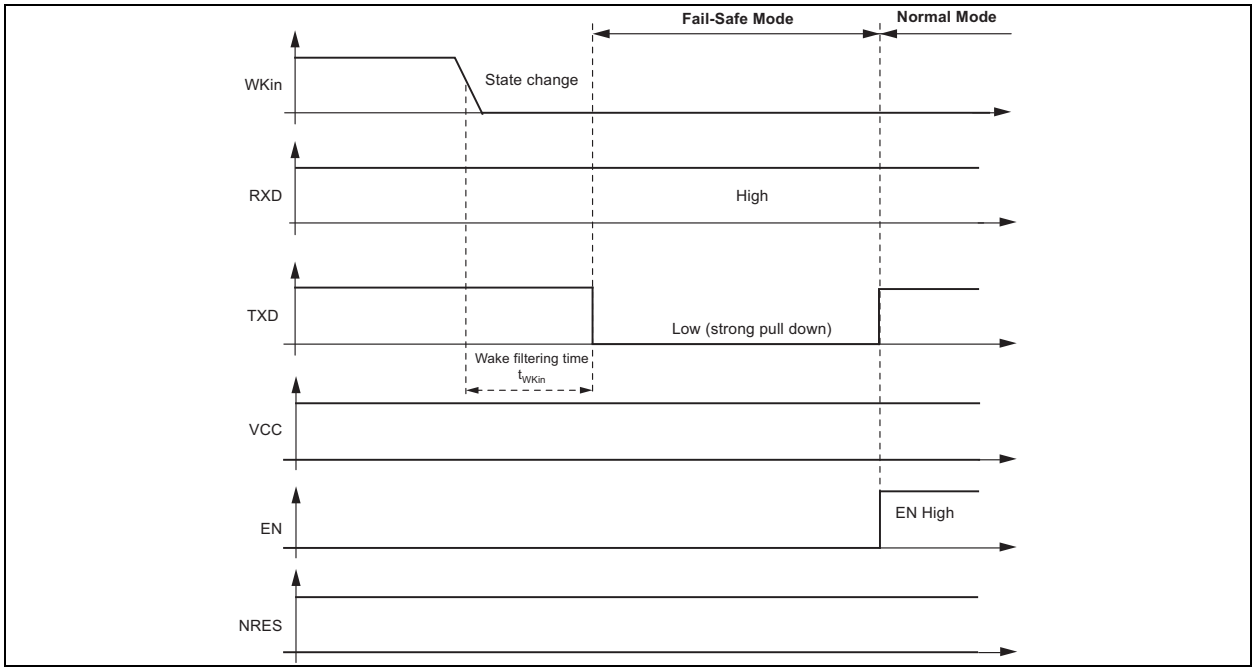


FIGURE 1-7: LOCAL WAKE-UP FROM SILENT MODE



1.3.3 WAKE-UP SOURCE RECOGNITION

The device can distinguish between different wake-up sources. Table 1-3. The wake-up source can be read on the TXD and RXD pins in Fail-Safe mode. These flags are immediately reset if the microcontroller sets the EN pin to high and the IC is in Normal mode.

TABLE 1-3: SIGNALING IN FAIL-SAFE MODE

Fail-Safe Sources	TXD	RXD
Bus wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin)	Low	High
$V_{VS\_th\_N\_F\_down}$ (battery) undervoltage detection (V_{VS} < 3.9V)	High	Low

1.4 Behavior under Low Supply Voltage Condition

After the battery voltage has been connected to the application circuit, the voltage at the VS pin increases according to the block capacitor (see Typical Application Circuit). If V_{VS} is higher than the minimum VS operation threshold $V_{VS\_th\_U\_F\_up}$,(typically 2.25V) the IC mode changes from Unpowered mode to Fail-Safe mode. As soon as V_{VS} exceeds the undervoltage threshold $V_{VS\_th\_F\_N\_up}$ (typically 4.6V), the LIN transceiver and the dual low side switches can be activated. The VCC output voltage reaches its nominal value after t_{VCC}. This parameter depends on the externally applied VCC capacitor and the load. The NRES output is low for the reset time delay t_{reset}. During this time t_{reset}, no mode change is possible.

The behavior of VCC, NRES and VS is shown in Figure 1-8, Figure 1-9, Figure 1-10 and Figure 1-11.

FIGURE 1-8: VCC AND NRES VERSUS VS (RAMP-UP) FOR 3.3V

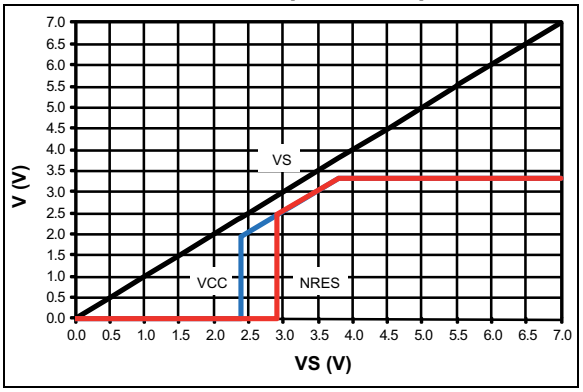


FIGURE 1-9: VCC AND NRES VERSUS VS (RAMP-DOWN) FOR 3.3V

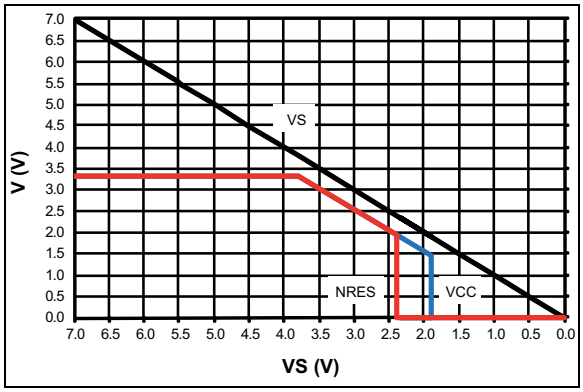


FIGURE 1-10: VCC AND NRES VERSUS VS (RAMP-UP) FOR 5V

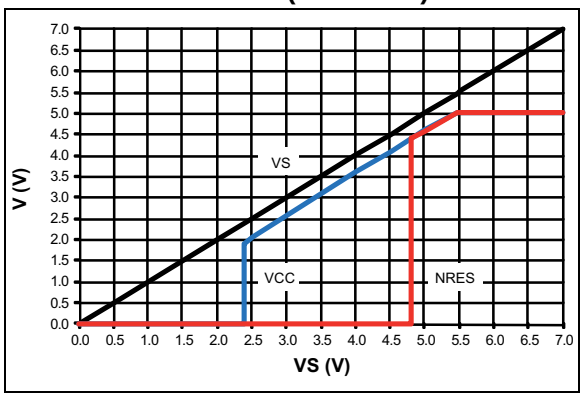
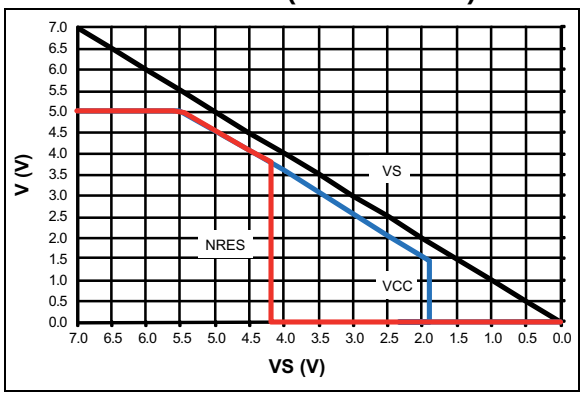


FIGURE 1-11: VCC AND NRES VERSUS VS (RAMP-DOWN) FOR 5V



The graphs are only valid if the VS ramp-up and ramp-down time is much slower than the VCC ramp-up time t_{VCC} and the NRES delay time t_{reset}.

If during Sleep mode the voltage level of V_{VS} drops below the undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typically 4.3V), the operation mode is not changed and no wake-up is possible. Only if the supply voltage on pin VS drops below the VS operation threshold $V_{VS\_th\_U\_down}$ (typically 2.05V), does the IC switch to Unpowered mode.

If during Silent mode the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$ the IC switches into Fail-Safe mode. If the supply voltage on pin VS drops below the VS operation threshold $V_{VS\_th\_U\_down}$ (typically 2.05V), does the IC switch to Unpowered mode.

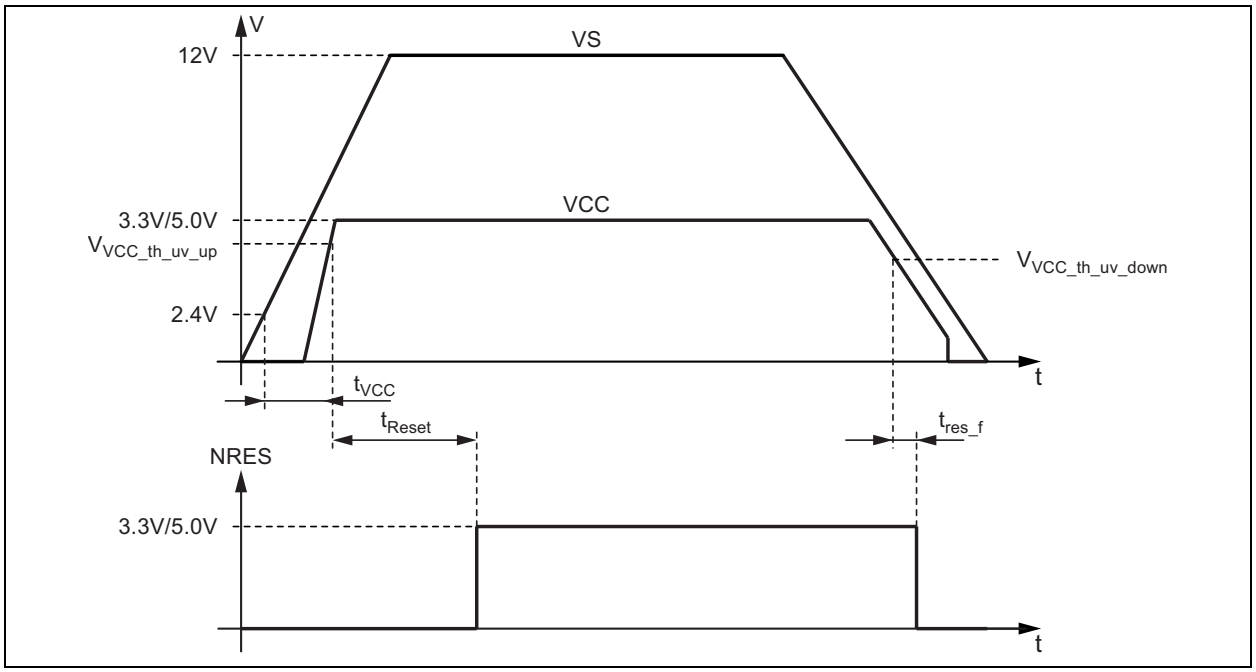
If during Normal mode the voltage level on pin VS drops below the VS undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typically 4.3V), the IC switches to Fail-Safe mode. This means the LIN transceiver and the dual low side drivers are disabled in order to avoid malfunctions or false bus messages. The voltage regulator remains active.

- For **ATA663331**: In this undervoltage situation it is possible to switch the device into Sleep mode or Silent mode by a falling edge at the EN input. This feature ensures that switching into these two current saving modes is always possible, allowing current consumption to be even further reduced. When the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$ (typically 2.6V) the IC switches into Fail-Safe mode.
- For **ATA663354**: Because of the VCC undervoltage condition in this situation, the IC is in Fail-Safe mode and can be switched into Sleep mode only. Only when the supply voltage V_{VS} drops below the operation threshold $V_{VS\_th\_U\_down}$ (typically 2.05V) does the IC switch into Unpowered mode.

The current consumption of the ATA6633XX in Silent mode or in Fail-Safe mode is always below 170 µA, even when the supply voltage V_{VS} is lower than the regulator's nominal output voltage V_{VCC}.

1.5 Voltage Regulator

FIGURE 1-12: VOLTAGE REGULATOR: SUPPLY VOLTAGE RAMP-UP AND RAMP-DOWN

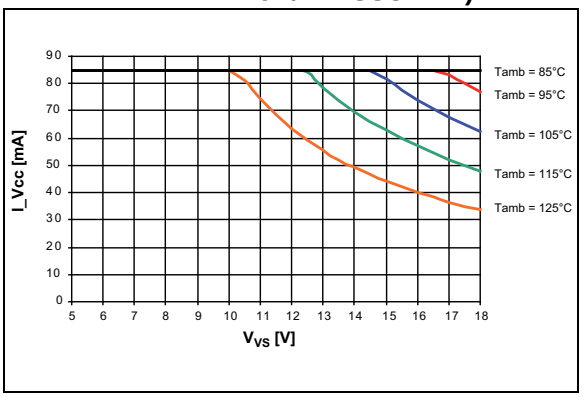


The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use a MLC capacitor with a minimum capacitance of 3.5 µF together with a 100 nF ceramic capacitor. Depending on the application, the values of these capacitors can be modified by the customer.

When the ATA6633XX is being soldered onto the PCB, it is mandatory to connect the exposed thermal pad with a wide GND plate on the printed board to achieve a good heat sink.

The main power dissipation of the IC is created from the VCC output current I_{VCC}, which is needed for the application. Figure 1-13 shows the safe operating area of the ATA6633XX without considering any output current of the drivers (LS1out, LS2out, HSout).

FIGURE 1-13: POWER DISSIPATION: SAFE OPERATING AREA: REGULATOR'S OUTPUT CURRENT I_{VCC} VERSUS SUPPLY VOLTAGE V_{VS} AT DIFFERENT AMBIENT TEMPERATURES (R_{thJA} = 45K/W ASSUMED)



1.6 Pin Descriptions

The descriptions of the pins are listed in Table 1-4.

TABLE 1-4: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1	RXD	Receive data output.
2	EN	Enables Normal mode if the input is high.
3	NRES	VCC undervoltage output, open drain, low at reset.
4	TXD	Transmit data input.
5	WKout	Low-voltage output to indicate local wake-up request.
6	LS1in	Low side 1 control input.
7	LS2in	Low side 2 control input.
8	HSin	High side control input.
9	HSout	High side output.
10	LS2out	Low side 2 output.
11	LS1out	Low side 1 output.
12	WKin	High-voltage input for local wake-up request.
13	GND	Ground.
14	LIN	LIN bus line input/output.
15	VS	Supply voltage.
16	VCC	Output voltage regulator 3.3V/5V/85 mA.
EP	EP	Exposed Thermal Pad (GND).

1.6.1 BUS DATA OUTPUT PIN (RXD)

In Normal mode, this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD; LIN low (dominant state) is reported by a low level at RXD. The output is a push-pull stage switching between VCC and GND. The AC characteristics are measured with an external load capacitor of 20 pF.

In Silent mode, the RXD output switches to high.

1.6.2 ENABLE INPUT PIN (EN)

The enable input pin controls the operation mode of the device. If EN is high, the circuit is in Normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V/5V/85 mA output capability.

If EN is switched to low while TXD is still high, the device is forced into Silent mode. No data transmission is then possible and the current consumption is reduced to $I_{VSsilent}$ typically 47 µA. The VCC regulator maintains full functionality.

If EN is switched to low while TXD is low, the device is forced into Sleep mode. No data transmission is possible and the voltage regulator is switched off.

Pin EN provides a pull down resistor to force the transceiver into Recessive mode if EN is disconnected.

1.6.3 UNDERVOLTAGE RESET OUTPUT PIN (NRES)

If the V_{VCC} voltage falls below the undervoltage detection threshold $V_{VCC\_th\_uv\_down}$, NRES switches to low after t_{res_f}. Even if V_{VCC} = 0V the NRES stays low because it is internally driven from the VS voltage. If VS voltage ramps down, NRES stays low until V_{VS} < 1.5V and then becomes high-impedant.

The undervoltage delay implemented keeps NRES low for t_{Reset} = 4 ms after V_{VCC} reaches its nominal value.

1.6.4 BUS DATA INPUT/OUTPUT (TXD)

In Normal mode, the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull up resistor), the LIN output transistor is turned off and the bus is in the recessive state. If the TXD pin stays at GND level while switching into Normal mode, it must be pulled to high level longer than 10 µs before the LIN driver can be activated. This feature prevents the bus line from being unintentionally driven to dominant state after Normal mode has been activated (also if a short circuit occurs at TXD to GND). If TXD is short circuited to GND, it is possible to switch to Sleep mode via the EN pin after t > t_{dom}.

In Fail-Safe mode, this pin is used as an output and signals the fail-safe source.

An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{dom} > 20 ms, the LIN bus driver is switched to the recessive state. Nevertheless, when switching to Sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (> 10 µs).

1.6.5 WAKE OUTPUT PIN (WKout)

The WKout pin is a low-voltage output used for waking up a microcontroller or other device. It is a push-pull output stage switching between VCC and GND. It is directly controlled by the WKin pin. If $V_{WKin} \geq V_{WKinH}$, WKout is low and no wake-up is detected. If $V_{WKin} < V_{WKinL}$, WKout is high and the device is switched into Fail-Safe mode if it was previously in a low power mode such as Sleep or Silent mode. Please note that during Silent, Fail-Safe and Normal mode, the output pin WKout is always showing the state of pin WKin.

If a local wake-up is not needed in the application, the WKout pin can be left open.

1.6.6 LOW-SIDE DRIVER PINS (LS1out, LS2out, LS1in, LS2in)

LS1out and LS2out are the low side driver outputs. They are only functional in Normal mode (See **Section 1.2 "Operating Modes"**). These outputs are both short circuit protected by means of output voltage monitoring and protected against overheating. They additionally include an active clamping circuitry to provide a freewheeling path needed for inductive loads. The clamping voltage $V_{LSclamp}$ is typically > 44V. Please note that an upper energy limit is defined both for single and for repetitive clamping events. This must be considered when choosing the load, because overheating caused by excessive clamping energy is not covered by the output protection and may therefore cause damage to the device.

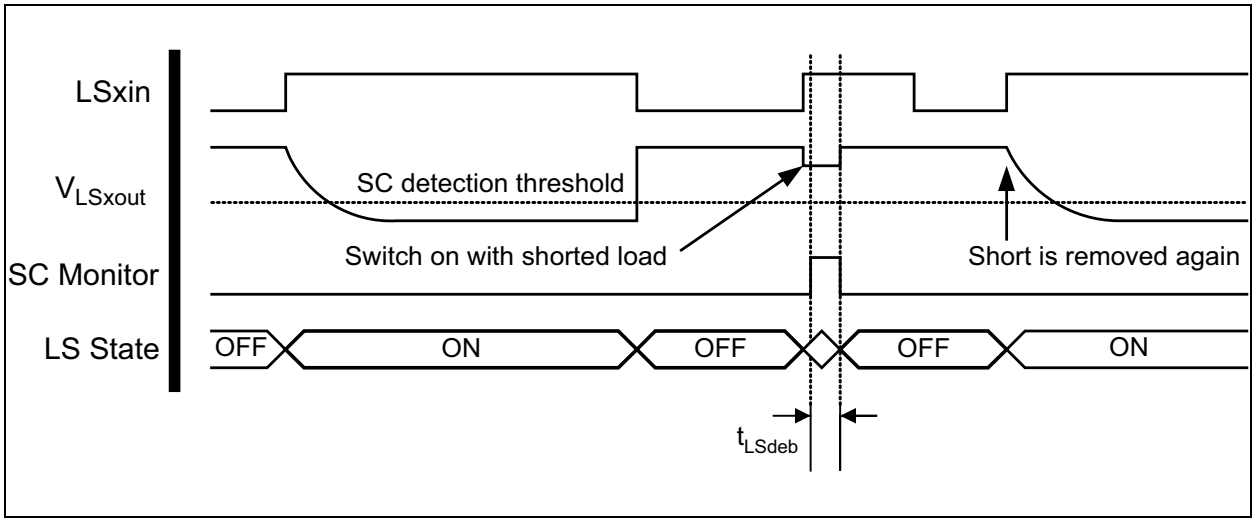
If the LS1in pin or the LS2in pin stay at GND level while switching into Normal mode, it must be pulled to high level longer than 10 µs before the low side driver can be activated. This feature prevents the low side drivers (LS1out pin or LS2out pin respectively) from being unintentionally switched on after Normal mode has been activated. To reactivate the low side drivers, switch LS1in or LS2in to high (> 10µs).

A disconnection of VS where the low sides are still supplied by VBAT through a load does not have any impact on the clamping feature. That is, voltages above the minimum clamping voltage level $V_{LSclamp}$ activate the energy freewheeling path within the low side transistor.

The low-side switches are controlled via the low-voltage input pins LS1in and LS2in. If the inputs are at high and the IC is in Normal mode (for example EN is high and there is no undervoltage supply condition), the outputs are switched on. For fail-safe reasons, both inputs are equipped with a pull-down resistor to GND. This will keep the low-side switches off in case of a missing connection from the controller.

If an overload condition is detected, the appropriate driver stage is shut down. The protective shutdown of the low side outputs is latched. That is, the corresponding control line LSxin has to go to low first before the output can be restarted again. Because the short circuit detection is done by means of drain-to-source voltage monitoring, the switch on event of the transistor is blanked out from the monitoring, so that a capacitor connected to the low-side output does not trigger the protection circuit upon activation of the transistor. See Figure 1-14.

FIGURE 1-14: SHORT CIRCUIT DETECTION TIMING



As can be seen in Figure 1-14, the output transistor is not switched on again until the control pin LSxin is switched off and on again by the microcontroller. The short circuit monitor is only enabled after the transistor reaches full conductivity. That is why the SC monitor line does not show any signal on the first and the last switching on event in Figure 1-14. Without a short present at the output, the transistor takes much more time to establish its operation point than if there is a short present.

1.6.7 HIGH-SIDE DRIVER PINS (HSOUT, HSIN)

This high-side switch is designed for low power loads such as LEDs, sensors or a voltage divider for measuring the supply voltage. It is functional in all operation modes of the chip but Sleep mode. Its structure is connected to the VS supply pin. This pin is protected against short circuits and also overheating.

The high-side switch is controlled via the low-voltage input pin HSin. If the input is at high, the output is switched on. For fail-safe reasons, the HSin input is equipped with a pull down resistor to GND. This keeps the high side switch off in case of a missing connection from the controller.

Please note that in case of a disconnected system ground, the module can be supplied via the connected load on the high-side output and an internal ESD structure. This is the case if the load has a different ground connection than the PCB. See **Section "Absolute Maximum Ratings†"** for current limits in such cases.

As is the case with low-side switches, the protective shutdown of the high-side output is debounced and latched. In other words, after a protective shutdown of the driver stage, the control line HSin has to go to low first before the output can be restarted.

1.6.8 WAKE INPUT PIN (WKin)

The WKin pin is a high-voltage input used to wake-up the device from Sleep mode or Silent mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically 10 µA is implemented. The voltage threshold for a wake-up signal is typically 2V below the VS voltage. If a local wake-up is not needed in the application, the WKin pin can be connected directly to the VS pin.

1.6.9 GROUND PIN (GND)

The IC does not affect the LIN bus in the event of GND disconnection. It can handle ground shifts of up to 11.5% with respect to V_{VS}.

1.6.10 BUS PIN (LIN)

A low-side driver is implemented with internal current limitation and thermal shutdown as well as an internal pull up resistor in compliance with LIN specification 2.x. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to VS, even in the event of a GND shift or supply disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification.

The fall time (transition from recessive to dominant state) and the rise time (transition from dominant to recessive state) are slope-controlled.

During a short circuit at the LIN pin to VBAT, the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. The VCC regulator works independently during LIN overtemperature switch off.

During a short circuit from LIN to GND the IC can be switched into Sleep or Silent mode and even in this case the current consumption is lower than 100 µA in Sleep mode and lower than 120 µA in Silent mode. If the short circuit disappears, the IC starts with a remote wake-up.

The reverse current is < 2 µA at pin LIN during loss of V_{VS}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.

1.6.11 SUPPLY PIN (VS)

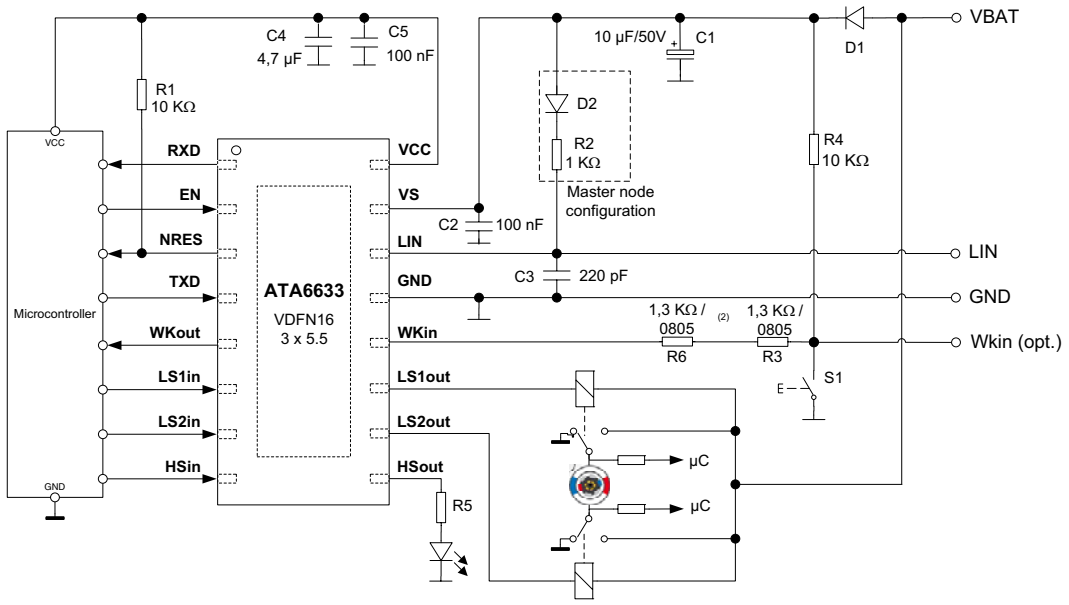
LIN operating voltage is V_{VS} = 5V to 28V. In order to avoid false bus messages, undervoltage detection is implemented to disable transmission if V_{VS} falls below typically 4.5V. After switching on V_{VS}, the IC starts in Fail-Safe mode and the voltage regulator is switched on.

The supply current in Sleep mode is typically 10 µA and 47 µA in Silent mode.

1.6.12 VOLTAGE REGULATOR OUTPUT PIN (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 85 mA, supplying the microcontroller and other ICs on the PCB, and is protected against overload by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and causes a reset signal at the NRES output pin if it drops below a defined threshold $V_{VCC\_th\_uv\_down}$.

Typical Application Circuit



Note 1: The Exposed Thermal Pad must always be connected to GND.

2: With these two resistors in series at the WKin- pin +/-6 kV ESD robustness according IEC61000-4-2 is achieved.

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage V_{VS}
DC Voltage ..... –0.3V to +40V
T_{amb} = 25°C, t_{Pulse} ≤ 500 ms, I_{VCC} ≤ 85 mA ..... –0.3V to + 43.5V
T_{amb} = 25°C, t_{Pulse} ≤ 2min, I_{VCC} ≤ 85 mA ..... –0.3V to + 28V
Logic Pin Voltage Levels (TXD, EN, HSin,LS1in, LS2in, NRES), V_{LOGIC} ..... –0.3V to + 5.5V
LIN Bus Levels V_{LIN}:
DC Voltage ..... –27V to +40V
Pulse Time < 500 ms ..... –27V to +43.5V
V_{VCC}:
DC Voltage ..... –0.3V to +5.5V
DC Input Current, I_{VCC} ..... –0.3mA to +200 mA
Logic Level Pins Injection Currents, t_{Pulse} ≤ 2min, I_{LOGIC} ..... –5 mA to +5 mA
HSout
DC Voltage, V_{HSout} ..... –0.3V to V_{VS} + 0.3V
DC Output Current, I_{HSout} ..... –50 mA
DC Current Injection Levels, V_{HSout} < 0V, V_{HSout} > V_{VS}, I_{HSout} ..... –20 mA to +10 mA
LS1out and LS2out
DC Voltage, V_{LSout} ..... –0.3V to V_{VS} + 42.5V
DC Output Current, I_{LSout} ..... –0.3mA to +250 mA
LS1out and LS2out Clamping Energies
Single Event, E_{AS} ..... +10 mJ
Repetitive (f ≤ 5 Hz), E_{AR} ..... +2 mJ
WKin Voltage Levels:
DC Voltage, V_{WKin} ..... –0.3V to +40V
Transient Voltage[(1)], V_{WKin} ..... –150V to +100V
ESD[(2)] Pin VS, WKin and LIN to GND (WKin with external circuitry according to applications diagram) ..... ± 6 kV
ESD[(3)] Pin HSout (100Ω Series Resistor, 22 nF to GND) to GND ..... ± 6 kV
ESD HBM Following STM5.1 with 1.5 kΩ/100 pF:
Pin VS, LIN, HSout to GND ..... ± 6 kV
Pin WKin to GND ..... ± 5 kV
Component Level ESD (HBM acc. ANSI/ESD STM5.1), JESD22-A114, AEC-Q100 (002) ..... ± 3 kV
CDM ESD STM 5.3.1 ..... ± 750 V
ESD Machine Model AEC-Q100-RevF(003) ..... ± 200 V
Virtual Junction Temperature, T_{vJ} ..... –40°C to +150°C
Storage Temperature, T_{stg} ..... –55°C to +150°C

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not ensured to function outside its operating ratings.

Note 1: According to ISO7637 (coupling 1 nF), with 2 x 1.3 KΩ.
2: According to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2.
3: According to ISO10605, with 330 pF/330Ω.

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
1	**VS Pin**						
1.1	Nominal DC Voltage Range	V_{VS}	5	13.5	28	V	
1.2	Supply Current in Sleep Mode	$I_{VSsleep}$	5	10	15	µA	Sleep mode $V_{LIN} > V_{VS} – 0.5V$ V_{VS} < 14V, T = 27°C (**Note 1**)
		$I_{VSsleep}$	3	11	18	µA	Sleep mode $V_{LIN} > V_{VS} – 0.5V$ V_{VS} < 14V
		$I_{VSsleep\_short}$	20	50	100	µA	Sleep mode V_{LIN} = 0V Bus shorted to GND V_{VS} < 14V
1.3	Supply Current in Silent Mode	$I_{VSsilent}$	30	47	58	µA	Bus recessive 5.5V < V_{VS} < 14V, all drivers off without load at VCC, T = 27°C (**Note 1**)
		$I_{VSsilent}$	30	50	64	µA	Bus recessive 5.5V < V_{VS} < 14V, all drivers off without load at VCC
		$I_{VSsilent}$	50	130	170	µA	Bus recessive 2V < V_{VS} < 5.5V, all drivers off without load at VCC
		$I_{VSsilent\_short}$	50	80	120	µA	Silent mode 5.5V < V_{VS} < 14V, all drivers off Bus shorted to GND without load at VCC
1.4	Supply Current in Normal Mode	I_{VSrec}	150	230	300	µA	Bus recessive V_{VS} < 14V, all drivers off without load at VCC
1.5	Supply Current in Normal Mode	I_{VSdom}	200	700	950	µA	Bus dominant (internal LIN pull up resistor active) V_{VS} < 14V without load at VCC
1.6	Supply current in Fail-Safe Mode	I_{VSfail}	40	55	80	µA	Bus recessive 5.5V < V_{VS} < 14V, all drivers off without load at VCC
		$I_{VSsilent}$	50	130	170	µA	Bus recessive 2V < V_{VS} < 5.5V, all drivers off without load at VCC
1.7	VS Undervoltage Threshold (Switching from Normal to Fail-Safe Mode)	$V_{VS\_th\_N\_F\_down}$	3.9	4.3	4.7	V	Decreasing supply voltage
		$V_{VS\_th\_F\_N\_up}$	4.1	4.6	4.9	V	Increasing supply voltage
1.8	VS Undervoltage Hysteresis	$V_{VS\_hys\_F\_N}$	0.1	0.25	0.4	V	
1.9	VS Operation Threshold (Switching to Unpowered Mode)	$V_{VS\_th\_U\_down}$	1.9	2.05	2.3	V	Switch to Unpowered mode
		$V_{VS\_th\_U\_F\_up}$	2.0	2.25	2.4	V	Switch from Unpowered to Fail-Safe mode

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
1.10	VS Undervoltage Hysteresis	$V_{VS\_hys\_U}$	0.1	0.2	0.3	V	
2	**RXD Output Pin**						
2.1	Low-Level Output Sink Capability	V_{RXDL}	—	0.2	0.4	V	Normal mode, V_{LIN} = 0V, I_{RXD} = 2 mA
2.2	High-Level Output Source Capability	V_{RXDH}	V_{VCC} – 0.4V	V_{VCC}– 0.2V	—	V	Normal mode V_{LIN} = V_{VS}, I_{RXD} = – 2mA
3	**TXD Input/Output Pin**						
3.1	Low-Level Voltage Input	V_{TXDL}	–0.3	—	+0.8	V	
3.2	High-Level Voltage Input	V_{TXDH}	2	—	V_{VCC} + 0.3V	V	
3.3	Pull-Up Resistor	R_{TXD}	40	70	100	kΩ	V_{TXD} = 0V
3.4	High-Level Leakage Current	I_{TXD}	–3	—	+3	µA	V_{TXD} = V_{VCC}
3.7	Low-Level Output Sink Current at LIN Wake-Up Request	I_{TXD}	2	2.5	8	mA	Fail-Safe mode V_{LIN} = V_{VS} , V_{WAKE} = 0V V_{TXD} = 0.4V
4	**EN Input Pin**						
4.1	Low-Level Voltage Input	V_{ENL}	–0.3	—	+0.8	V	
4.2	High-Level Voltage Input	V_{ENH}	2	—	V_{VCC} + 0.3V	V	
4.3	Pull-Down Resistor	R_{EN}	50	125	200	kΩ	V_{EN} = V_{VCC}
4.4	Low-Level Input Current	I_{EN}	–3	—	+3	µA	V_{EN} = 0V
5	**NRES Open Drain Output Pin**						
5.1	Low-Level Output Voltage	V_{NRESL}	—	0.2	0.4	V	V_{VS} ≥ 5.5V I_{NRES} = 2 mA
5.2	Undervoltage Reset Time	t_{Reset}	2	4	6	ms	V_{VS} ≥ 5.5V C_{NRES} = 20 pF
5.3	Reset Debounce Time for Falling Edge	t_{res_f}	0.5	—	10	µs	V_{VS} ≥ 5.5V C_{NRES} = 20 pF
5.4	Switch Off Leakage Current	I_{NRES_L}	–3	—	+3	µA	$V_{NRES = 5.5V}$
6	**VCC Voltage Regulator ATA663331**						
6.1	Output Voltage VCC	V_{VCCnor}	3.234	—	3.366	V	4V < V_{VS} < 18V (0 mA to 50 mA)
		V_{VCCnor}	3.234	—	3.366	V	4.5V < V_{VS} < 18V (0 mA to 85 mA) (**Note 2**)
6.2	Output Voltage V_{VCC} at Low V_{VS}	V_{VCClow}	V_{VS} – V_D	—	3.366	V	3V < V_{VS} < 4V

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
6.3	Regulator Drop Voltage	V_{D1}	—	100	150	mV	V_{VS} > 3V, I_{VCC} = –15 mA
6.4	Regulator Drop Voltage	V_{D2}	—	300	500	mV	V_{VS} > 3V, I_{VCC} = –50 mA
6.5	Line Regulation Maximum	VCC_{line}	—	0.1	0.2	%	4V < V_{VS} < 18V
6.6	Load Regulation Maximum	VCC_{load}	—	0.1	0.5	%	5 mA < I_{VCC} < 50 mA
6.7	Output Current Limitation	I_{VCClim}	—	–180	–120	mA	V_{VS} > 4V
6.8	Load Capacity	C_{load}	3.5	4.7	—	µF	MLC capacitor (**Note 3**)
6.9	VCC Undervoltage Threshold (NRES ON)	$V_{VCC\_th\_uv\_down}$	2.3	2.6	2.8	V	Referred to VCC V_{VS} > 4V
	VCC Undervoltage Threshold (NRES OFF)	$V_{VCC\_th\_uv\_up}$	2.4	2.7	2.9	V	Referred to VCC V_{VS} > 4V
6.10	Hysteresis of VCC Undervoltage Threshold	$V_{VCC\_hys\_uv}$	100	200	300	mV	Referred to VCC V_{VS} > 4V
6.11	Ramp-Up time V_{VS} > 4V to V_{VCC} = 3.3V	t_{VCC}	—	1	1.5	ms	C_{VCC} = 4.7 µF I_{load} = –5 mA at VCC
7	**VCC Voltage Regulator ATA663354**						
7.1	Output Voltage VCC	V_{VCCnor}	4.9	—	5.1	V	5.5V < V_{VS} < 18V (0 mA to 50 mA)
		V_{VCCnor}	4.9	—	5.1	V	6V < V_{VS} < 18V (0 mA to 85 mA) (**Note 2**)
7.2	Output Voltage V_{VCC} at Low V_{VS}	V_{VCClow}	V_{VS} – V_D	—	5.1	V	4V < V_{VS} < 5.5V
7.3	Regulator Drop Voltage	V_{D1}	—	100	200	mV	V_{VS} > 4V, I_{VCC} = –20 mA
7.4	Regulator Drop Voltage	V_{D2}	—	300	500	mV	V_{VS} > 4V, I_{VCC} = –50 mA
7.5	Regulator Drop Voltage	V_{D3}	—	—	150	mV	V_{VS} > 3.3V, I_{VCC} = –15 mA
7.6	Line Regulation Maximum	VCC_{line}	—	0.1	0.2	%	5.5V < V_{VS} < 18V
7.7	Load Regulation Maximum	VCC_{load}	—	0.1	0.5	%	5 mA < I_{VCC} < 50 mA
7.8	Output Current Limitation	I_{VCClim}	—	–180	–120	mA	V_{VS} > 5.5V
7.9	Load Capacity	C_{load}	3.5	4.7	—	µF	MLC capacitor (**Note 3**)

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
7.10	VCC Undervoltage Threshold (NRES ON)	$V_{VCC\_th\_uv\_down}$	4.2	4.4	4.6	V	Referred to VCC V_{VS} > 4V
	VCC Undervoltage Threshold (NRES OFF)	$V_{VCC\_hys\_uv}$	4.3	4.6	4.8	V	Referred to VCC V_{VS} > 4V
7.11	Hysteresis of Undervoltage Threshold	$V_{VCC\_hys\_uv}$	100	200	300	mV	Referred to VCC V_{VS} > 5.5V
7.12	Ramp-Up Time V_{VS} > 5.5V to V_{VCC} = 5V	t_{VCC}	—	1	1.5	ms	C_{VCC} = 4.7 µF I_{load} = –5 mA at VCC
8	**LIN Bus Driver: Bus Load Conditions: Load 1 (Small): 1 nF, 1 kΩ; Load 2 (Large): 10 nF, 500Ω;; C_{RXD} = 20 pF, Load 3 (Medium): 6.8 nF, 660Ω characterized on samples 10.7 and 10.8 specifies the timing parameters for proper operation at 20 kBit/s and 10.9 kBit/s and 10.10 kBit/s at 10.4 kBit/s**						
8.1	Driver Recessive Output Voltage	V_{BUSrec}	0.9 * V_{VS}	—	V_{VS}	V	Load1/Load2
8.2	Driver Dominant Voltage	$V_{\_LoSUP}$	—	—	1.2	V	V_{VS} = 7V R_{load} = 500Ω
8.3	Driver Dominant Voltage	$V_{\_HiSUP}$	—	—	2	V	V_{VS} = 18V R_{load} = 500Ω
8.4	Driver Dominant Voltage	$V_{\_LoSUP\_1k}$	0.6	—	—	V	V_{VS} = 7V R_{load} = 1000Ω
8.5	Driver Dominant Voltage	$V_{\_HiSUP\_1k}$	0.8	—	—	V	V_{VS} = 18V R_{load} = 1000Ω
8.6	Pull-Up Resistor to V_{VS}	R_{LIN}	20	30	47	kΩ	The serial diode is mandatory
8.7	Voltage Drop at the Serial Diodes	$V_{SerDiode}$	0.4	—	1.0	V	In pull up path with R_{slave} $I_{SerDiode}$ = 10 mA (**Note 3**)
8.8	LIN Current Limitation V_{BUS} = V_{Bat_max}	I_{BUS_LIM}	40	120	200	mA	
8.9	Input Leakage Current at the Receiver Including Pull-Up Resistor as Specified	$I_{BUS\_PAS\_dom}$	–1	–0.35	—	mA	Input leakage current Driver off V_{BUS} = 0V V_{VS} = 12V
8.10	Leakage Current LIN Recessive	$I_{BUS\_PAS\_rec}$	—	10	20	µA	Driver off 8V < V_{VS} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{VS}$

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
8.11	Leakage Current when Control Unit Disconnected from Ground. Loss of local ground must not affect communication in the residual network.	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	$GND_{Device} = V_{VS}$ V_{VS} = 12V 0V < V_{BUS} < 18V
8.12	Leakage Current at Disconnected Battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	$I_{BUS\_NO\_bat}$	—	0.1	2	µA	V_{VS} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V
8.13	Capacitance on pin LIN to GND	C_{LIN}	—	—	20	pF	Note 3
9	**LIN Bus Receiver**						
9.1	Center of Receiver Threshold	V_{BUS_CNT}	0.475 * V_{VS}	0.5 * V_{VS}	0.525 * V_{VS}	V	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$
9.2	Receiver Dominant State	V_{BUSdom}	–27	—	0.4 * V_{VS}	V	V_{EN} = 5V/3.3V
9.3	Receiver Recessive State	V_{BUSrec}	0.6 * V_{VS}	—	40	V	V_{EN} = 5V/3.3V
9.4	Receiver Input Hysteresis	V_{BUShys}	0.028 * V_{VS}	0.1 * V_{VS}	0.175 * V_{VS}	V	$V_{hys} = V_{th\_rec} – V_{th\_dom}$
9.5	Pre-Wake Detection LIN High Level Input Voltage	V_{LINH}	V_{VS} – 2V	—	V_{VS} + 0.3V	V	
9.6	Pre-Wake Detection LIN Low Level Input Voltage	V_{LINL}	–27	—	V_{VS} – 0.3V	V	Activates the LIN receiver
10	**Internal Timers**						
10.1	Dominant Time for Wake-Up via LIN Bus	t_{bus}	50	100	150	µs	V_{LIN} = 0V
10.2	Time Delay for Mode Change from Fail-Safe mode to Normal Mode via the EN Pin	t_{norm}	5	15	20	µs	V_{EN} = 5V/3.3V
10.3	Time Delay for Mode Change from Normal Mode to Sleep Mode via the EN Pin	t_{sleep}	5	15	20	µs	V_{EN} = 0V

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
10.4	TXD Dominant Time-Out Time	t_{dom}	20	40	60	ms	V_{TXD} = 0V
10.6	Time Delay for Mode Change from Silent Mode to Normal Mode via the EN Pin	t_{s_n}	5	15	40	µs	V_{EN} = 5V/3.3V
10.7	Duty Cycle 1	D1	0.396	—	—	—	$TH_{Rec(max)}$ = 0.744 * V_{VS} $TH_{Dom(max)}$ = 0.581 * V_{VS} V_{VS} = 7.0V to 18V t_{Bit} = 50 µs D1 = $t_{bus\_rec(min)}$/(2 * t_{Bit})
10.8	Duty Cycle 2	D2	—	—	0.581	—	$TH_{Rec(min)}$ = 0.422 * V_{VS} $TH_{Dom(min)}$ = 0.284 * V_{VS} V_{VS} = 7.6V to 18V t_{Bit} = 50 µs D2 = $t_{bus\_rec(max)}$/(2 * t_{Bit})
10.9	Duty Cycle 3	D3	0.417	—	—	—	$TH_{Rec(max)}$ = 0.778 * V_{VS} $TH_{Dom(max)}$ = 0.616 * V_{VS} V_{VS} = 7.0V to 18V t_{Bit} = 96 µs D3 = $t_{bus\_rec(min)}$/(2 * t_{Bit})
10.10	Duty Cycle 4	D4	—	—	0.590	—	$T_{HRec(min)}$ = 0.389 * V_{VS} $T_{HDom(min)}$ = 0.251 * V_{VS} V_{VS} = 7.6V to 18V t_{Bit} = 96 µs D4 = $t_{bus\_rec(max)}$/(2 * t_{Bit})
10.11	Slope Time Falling and Rising Edge at LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5	—	22.5	µs	V_{VS} = 7.0V to 18V
10.12	TXD Release Time after Dominant Time-Out Detection	t_{DTOrel}	10	—	20	µs	Note 1
11	**Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: C_{RXD} = 20 pF**						
11.1	Propagation Delay of Receiver	t_{rx_pd}	—	—	6	µs	V_{VS} = 7V to 18V t_{rx_pd} = $max_{(trx\_pdr, trx\_pdf)}$
11.2	Symmetry of Receiver Propagation Delay Rising Edge Minus Falling Edge	t_{rx_sym}	–2	—	+2	µs	V_{VS} = 7V to 18V t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}
12	**WKin Pin**						
12.1	High-Level Input Voltage	V_{WKinH}	V_{VS} – 1V	—	V_{VS} + 0.3V	V	
12.2	Low-Level Input Voltage	V_{WKinL}	–1	—	V_{VS} –3.3V	V	Initializes a wake-up signal
12.3	WKin Pull-Up Current	I_{WKin}	–30	–10	–3	µA	V_{VS} < 28V, V_{WKin} = 0V

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
12.4	High-Level Leakage Current	I_{WKinL}	–5	—	+5	µA	V_{VS} = 28V, V_{WKin} = 28V
12.5	Debounce Time of Low Pulse for Wake-Up via WKin Pin	t_{WKin}	50	100	150	µs	V_{WKin} = 0V
13	**WKout Pin**						
13.1	Low-Level Output Sink Capability	V_{WKoutL}		0.2	0.4	V	V_{WKin} = V_{VS} I_{WKout} = 2 mA
13.2	High-Level Output Source Capability	V_{WKoutH}	V_{VCC} – 0.4V	V_{VCC}– 0.2V	—	V	V_{WKin} = 0V I_{WKout} = –2 mA
14	**LS1out, LS2out Pins**						
14.1	Output Drain-to-Source on Resistance	$R_{DSon,LS}$	—	—	3	Ω	I_{LSout} = 100 mA
14.2	Leakage Current	I_{LSleak}	—	—	10		–0.2V < V_{LSout} < 40V
14.3	Active Clamping Voltage	$V_{LSclamp}$	43	44	48	V	I_{LSout} = 20mA
14.4	Short Circuit Detection Threshold	V_{SCth_LS}	1.25	1.5	1.75	V	5.5V < V_{VS} < 28V
14.9	Switch On Slope (Fall Time)	$t_{LSslope,fall}$	5	—	20	µs	V_{VS} = 16V R_{load} = 100Ω C_{load} = 1 nF transition from 80% down to 20% of V_{VS}
14.10	Switch Off Slope (Rise Time)	$t_{LSslope,rise}$	5	—	20	µs	V_{VS} = 16V R_{load} = 100Ω C_{load} = 1 nF transition from 20% to 80% of V_{VS}
14.11	Switch On Delay	t_{LSdel}	5	—	30	µs	V_{VS} = 16V R_{load} = 100Ω C_{load} = 1 nF time from LSin = high to V_{LSout} = 50% of V_{VS}
14.12	Switch Off Delay	t_{LSdel}	20	—	50	µs	V_{VS} = 16V R_{load} = 100Ω C_{load} = 1 nF time from LSin = low to V_{LSout} = 50% of V_{VS}
14.13	Short Circuit Detection Debouncing Time	t_{Lsdeb}	2	3.75	10	µs	Note 1

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
15	**LS1in, LS2in Pins**						
15.1	Low-Level Voltage Input	V_{LSin_L}	–0.3	—	$0.3V_{VC}$	V	
15.2	High-Level Voltage Input	V_{LSin_H}	$0.7V_{VC}$	—	V_{VCC} + 0.3	V	
15.3	Pull-Down Resistor	R_{LSin}	50	100	150	kΩ	V_{LSin} = V_{VCC}
15.4	Low-Level Input Current	I_{LSin}	–1	—	+1	µA	V_{LSin} = 0V
15.5	Maximum Switching Frequency	$f_{LSin,max}$	1	—	—	kHz	$R_{Load,LSxout}$ ≥ 100Ω $L_{Load,LSxout}$ ≤ 1 mH (**Note 3**)
16	**HSout pin**						
16.1	Output Drain-to-Source on Resistance	$R_{DSon,HS}$	—	—	20	Ω	I_{HSout} = –20 mA
16.2	Leakage Current	$I_{leak,HS}$	—	—	2	µA	–0.2V < V_{HSout} < V_{VS} + 0.2V
16.5	Switch Off Slope (Fall Time)	$t_{HSslope,fall}$	0.5	—	5	µs	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1 nF transition from 80% down to 20% of V_{VS}
16.6	Switch On Slope (Rise Time)	$t_{HSslope,rise}$	0.5	—	5	µs	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1 nF transition from 20% to 80% of V_{VS}
16.7	Switch On Delay	t_{HSdel}	3	—	20	µs	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1 nF time from HSin = HIGH to V_{HSout} = 50% of V_{VS}
16.8	Switch Off Delay	t_{HSdel}	3	—	20	µs	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1 nF time from HSin = LOW to V_{HSout} = 50% of V_{VS}
16.9	Short Circuit Detection Threshold	V_{SCth_HS}	V_{VS} – 6V	—	V_{VS} – 2V	V	
16.10	Short Circuit Deb. Time	t_{HS_deb}	2	—	10	µs	
17	**HSin Pin**						
17.1	Low-Level Voltage Input	V_{HSin_L}	–0.3	—	$0.3V_{VC}$	V	
17.2	High-Level Voltage Input	V_{HSin_H}	$0.7V_{VC}$	—	V_{VCC} + 0.3	V	
17.3	Pull-Down Resistor	R_{HSin}	50	100	150	kΩ	V_{HSin} = V_{VCC}

Note 1: 100% correlation tested.

2: Characterized on samples.

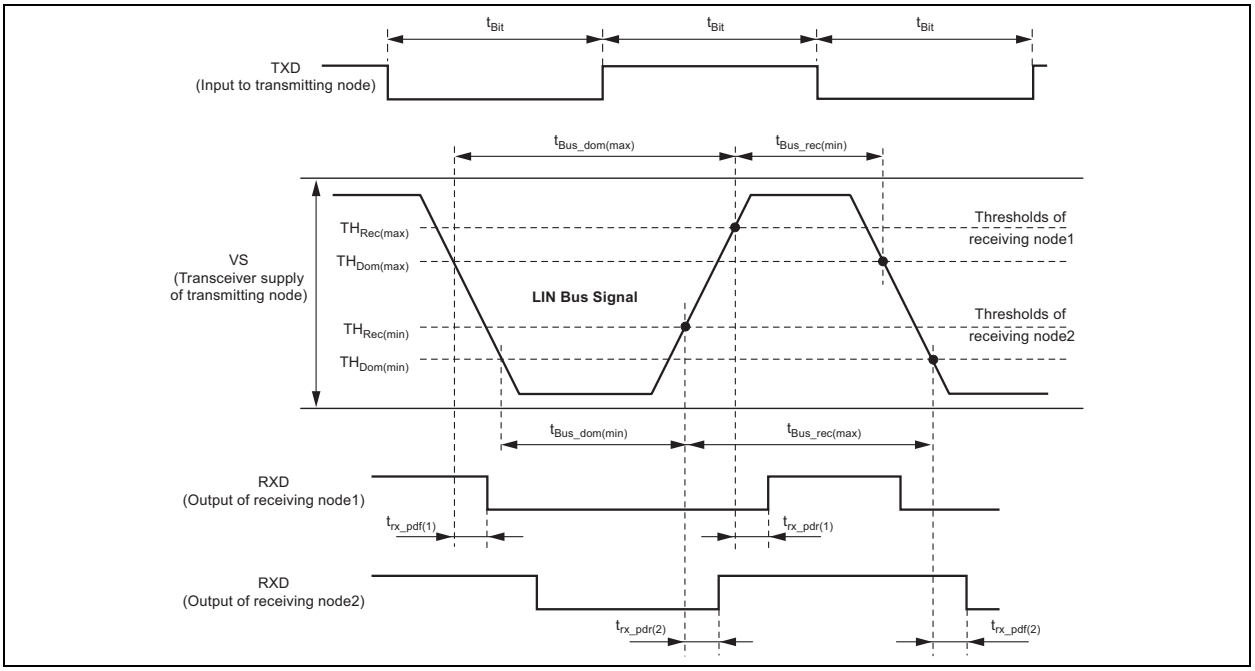
3: Design parameter.

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
17.4	Low-Level Input Current	I_{HSin}	–1	—	+1	µA	V_{HSin} = 0V
17.5	Maximum Switching Frequency	$f_{HSin,max}$	5	—	—	kHz	R_{Load} = 560Ω (**Note 3**)

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.

FIGURE 2-1: DEFINITION OF BUS TIMING CHARACTERISTICS



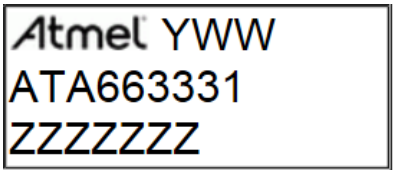
TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Thermal Resistance Virtual Junction to Exposed Thermal Pad	R_{thvJC}	—	+8	—	K/W	
Thermal Resistance Virtual Junction to Ambient, where Exposed Thermal Pad is Soldered to PCB According to JEDEC	R_{thvJA}	—	+45	—	K/W	
Thermal Shutdown of VCC Regulator	T_{VCCoff}	+150	+165	+180	°C	
Thermal Shutdown of LIN Output	T_{LINoff}	+150	+165	+180	°C	
Thermal Shutdown of Driver Stages	T_{DSoff}	+150	+165	+180	°C	
Thermal Shutdown Hysteresis	T_{hys}	—	+10	—	°C	

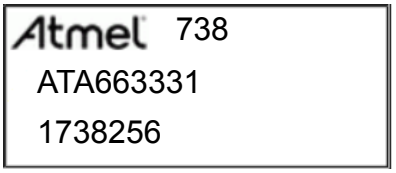
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

16-Lead 3 x 5.5 mm VDFN



Example

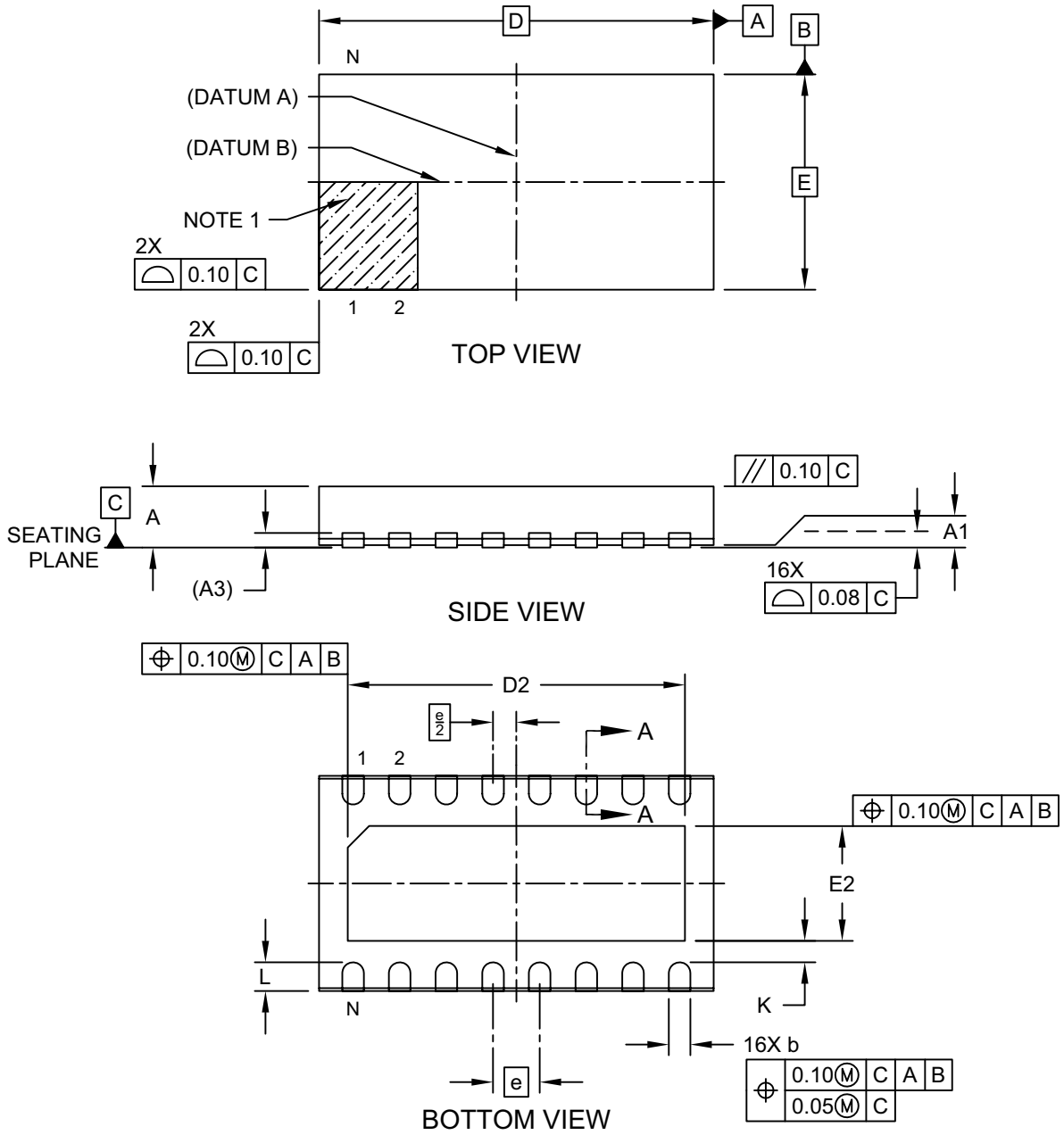


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead Very Thin Plastic Dual Flat, No Lead Package (QDB) - 5.5x3 mm Body [VDFN] With Stepped Wettable Flanks and 4.7x1.6 mm Exposed Pad

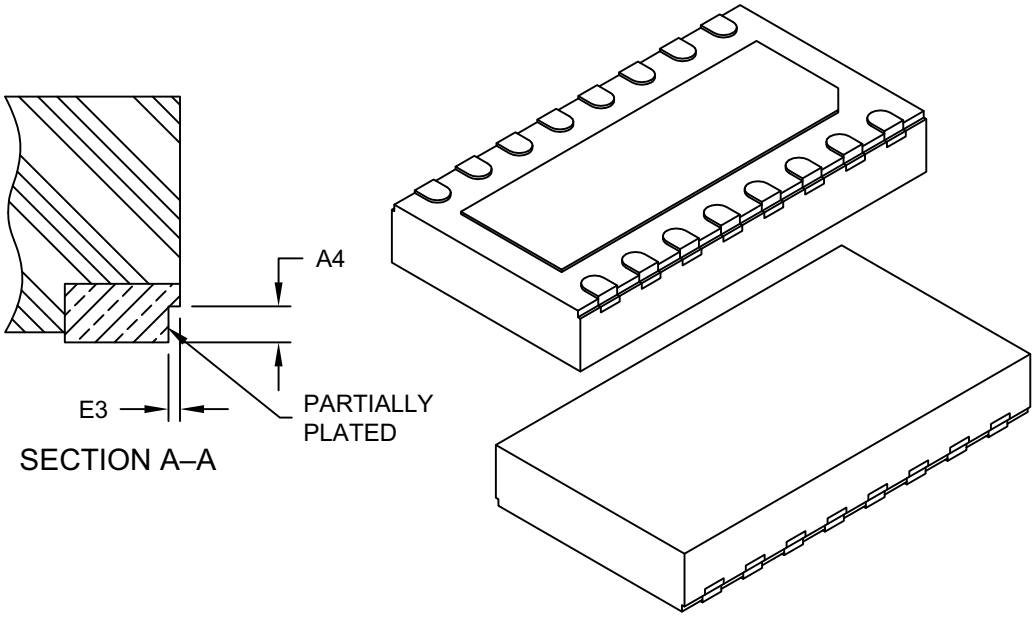
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21363 Rev A Sheet 1 of 2

16-Lead Very Thin Plastic Dual Flat, No Lead Package (QDB) - 5.5x3 mm Body [VDFN] With Stepped Wettable Flanks and 4.7x1.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Wettable Flank Step Cut Depth	A4	0.10	0.13	0.15
Overall Length	D		5.50 BSC	
Exposed Pad Length	D2	4.60	4.70	4.80
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Wettable Flank Step Cut Width	E3	-	-	0.04
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

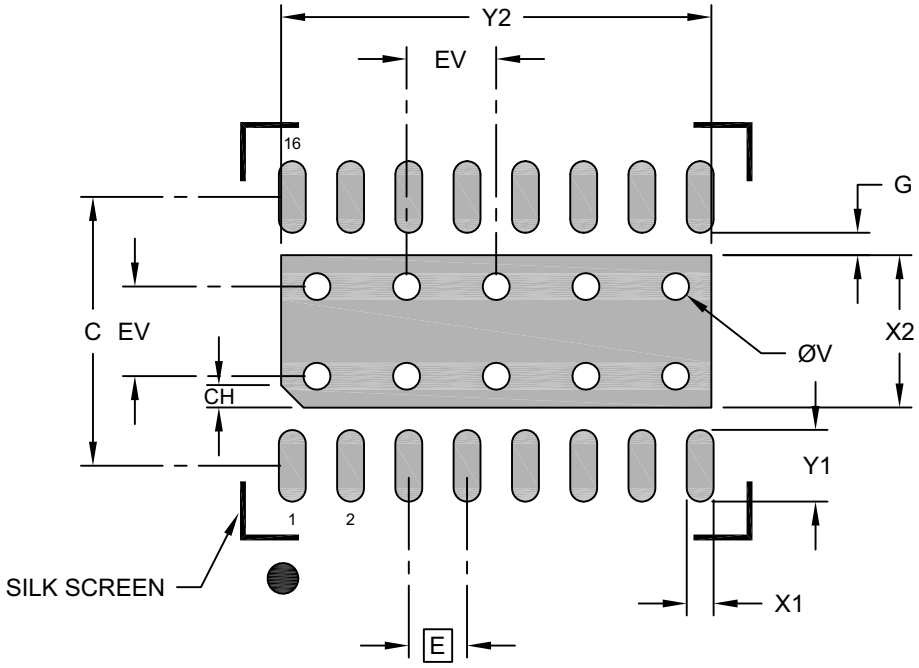
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21363 Rev A Sheet 2 of 2

16-Lead Very Thin Plastic Dual Flat, No Lead Package (QDB) - 5.5x3 mm Body [VDFN] With Stepped Wettable Flanks and 4.7x1.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			4.80
Contact Pad Spacing	CH		0.25	
Exposed Pad 45° Corner Chamfer	C		3.00	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.80
Contact Pad to Center Pad (X16)	G	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23363 Rev A

APPENDIX A: REVISION HISTORY

Revision A (November 2017)

- Original Release of this Document.
- This Document Replaces Atmel - 9231A–AUTO–08/15.
- Updated the Typical Application Circuit.
- Minor text updates.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	[X](1)	X
Device	Package	Tape and Reel Option	Package Directives Classification

Device:	ATA663331:		LIN System Basis Chip Including LIN Transceiver, 3.3V Voltage Regulator, Dual Low Side Driver and a High Side Switch
	ATA663354:		LIN System Basis Chip Including LIN Transceiver, 5V Voltage Regulator, Dual Low Side Driver and a High Side Switch
Package:	GD	=	16-Lead VDFN
Tape and Reel Option:	Q	=	330 mm diameter Tape and Reel
Package Directives Classification:	W	=	Package according to RoHS(2)

Examples:

a) ATA663331-GDQW: ATA663331, 16-Lead VDFN, Tape and Reel, Package according to RoHS

b) ATA663354-GDQW: ATA663354, 16-Lead VDFN, Tape and Reel, Package according to RoHS

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: RoHS compliant, Maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl) and less than 0.15% (1500 ppm) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

NOTES:

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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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