

## Four-Channel CMOS LDO with Select Mode, Shutdown and Independent Reset

### Features

- Four Independent 150 mA LDOs
- Low Supply Current (220  $\mu$ A typical)
- High Output Voltage Accuracy (0.5% typical)
- Low Dropout Voltage (100 mV typical with 150 mA load)
- Four Independent Shutdown Inputs
- Select Mode™: Selectable Output Voltages for High Design Flexibility
- Integrated Independent Microprocessor Reset
- Low Noise Outputs
- Fast Response from Shutdown (10  $\mu$ s typical)
- RESET Output for Low Battery Detection or Reset Generator
- Over Current and Over-Temperature Protection
- Small 16-Pin QSOP Package
- Specified Junction Temperature Range:
  - -40°C to +125°C

### Applications

- Battery Operated Systems
- Potable Computers
- Set Top Boxes
- Load Partitioning
- Medical Instruments
- Cellular / GSM / PHS Phones
- Instrumentation
- Linear Post Regulator for SMPS
- Pagers

### Description

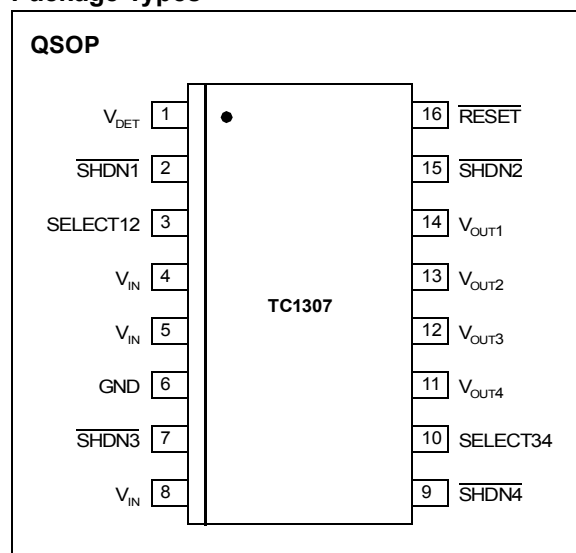
The TC1307 combines four CMOS Low Dropout Linear Regulators with a Microcontroller Monitor in a space-saving 16-Pin QSOP package. Developed specifically for battery powered portable applications, all four outputs of the TC1307 typically consume a total of 220  $\mu$ A supply current, hold the output voltage to a tolerance of 0.5% and require 100 mV of headroom for regulation at the maximum output current of 150 mA. In addition to the four high performance LDOs, the TC1307 also includes a voltage detector with a delayed RESET output that can be configured for low battery detection or Microcontroller Reset Generator.

All four LDOs have independent shutdown inputs and can be programmed using two select inputs making the TC1307 adaptable for a wide range of multiple output applications. The tri-state SELECT12 input pin allows the designer to select the output voltages on  $V_{OUT1}$ , and  $V_{OUT2}$  from three different values (2.5V, 2.8V or 3.0V). The tri-state SELECT34 input pin allows the designer to select the output voltages on  $V_{OUT3}$ , and  $V_{OUT4}$  from three different values (1.8V, 2.5V or 2.8V). All four LDO's require only a 1  $\mu$ F output capacitor for stability that can be ceramic, tantalum or aluminum over the entire input voltage operating range and 0 mA to 150 mA rated load range. All four LDOs have low output noise and excellent dynamic response when faced with sudden line and load changes.

The voltage detect pin is set for a threshold of 2.63V (typical) and operates down to a minimum input voltage of 1.0V. When the voltage on the detect pin rises above the 2.63V threshold, the RESET output is held low for 300 ms (typical).

Additional integrated features include over-current protection and over-temperature protection providing full protection from external load faults.

### Package Types



## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Maximum Ratings\*

$V_{DD}$ .....6.5V  
 All inputs and outputs w.r.t. .... $V_{IN} + 0.3V$  to  $-0.3V$   
 Output Short Circuit Current .....continuous  
 Storage temperature.....  $-65^{\circ}C$  to  $+150^{\circ}C$   
 Operating Junction Temperature,  
 $T_J$ ..... $-40^{\circ}C < T_J < +150^{\circ}C$   
 Maximum Junction Temperature,  $T_J$ ..... $150^{\circ}C$   
 ESD protection on all pins..... $\geq 4$  kV

**\*Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## PIN FUNCTION TABLE

Name	Function
$V_{DET}$	Voltage Detect Input
SHDN1	Shutdown for $V_{OUT1}$
SELECT12	Input for setting $V_{OUT1}$ and $V_{OUT2}$ .
$V_{IN}$	Input Voltage Connection
$V_{IN}$	Input Voltage Connection
GND	Ground connection
SHDN3	Shutdown for $V_{OUT3}$
$V_{IN}$	Input Voltage Connection
SHDN4	Shutdown for $V_{OUT4}$
SELECT34	Input for setting $V_{OUT3}$ and $V_{OUT4}$ .
$V_{OUT4}$	LDO4 Output
$V_{OUT3}$	LDO3 Output
$V_{OUT2}$	LDO2 Output
$V_{OUT1}$	LDO1 Output
SHDN2	Shutdown for $V_{OUT2}$
RESET	Reset Output

## ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are established for  $V_{IN} = V_R + 1$ ,  $I_L = 100 \mu A$ ,  $C_L = 3.3 \mu F$ ,  $\overline{SHDN} > V_{IH}$ ,  $T_A = 25^{\circ}C$ .  
**Boldface** type specifications apply for junction temperatures,  $T_J$  (**Note 9**) of  $-40^{\circ}C$  to  $+125^{\circ}C$ .

Parameter	Sym	Min	Typ	Max	Units	Conditions
<b>Input Characteristics:</b>						
Input Operating Voltage	$V_{IN}$	<b>2.7</b>	—	<b>6.0</b>	V	<b>Note 1</b>
Input Quiescent Current	$I_{IN}$	—	220	<b>370</b>	$\mu A$	$\overline{SHDN} = V_{IH}$ , $I_L = 0$
Input Shutdown Current	$I_{IN\_SHDN}$	—	0.1	0.5	$\mu A$	$\overline{SHDN} = 0V$
<b>Output Characteristics:</b>						
Maximum Output Current	$I_{OUT\_MAX}$	<b>150</b>	—	—	mA	
Output Short Circuit Current (Average)	$I_{OUT\_SC}$	—	360	—	mA	$V_{OUT} = 0V$
Voltage Regulation LDO1/LDO2/LDO3/LDO4	$V_{OUT}$	<b><math>V_R - 2.5\%</math></b>	$V_R \pm 0.5$	<b><math>V_R + 2.5\%</math></b>	V	<b>Note 2</b>

- Note 1:** The minimum  $V_{IN}$  must meet two conditions:  $V_{IN} \geq 2.7V$  and  $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$ .  
**2:**  $V_R$  is the nominal regulator output voltage. For example:  $V_R = 1.8V, 2.5V, 2.8V$  or  $3.0V$ .  
**3:**  $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$ ,  $V_{OUT-HIGH}$  = Highest voltage measured over the temperature range.  $V_{OUT-LOW}$  = Lowest voltage measured over the temperature range.  
**4:** Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1mA to the maximum specified output current. Changes in output voltage due to heating effects are determined using thermal regulation specification  $TCV_{OUT}$ .  
**5:** Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied. Specifications are for a current pulse equal to  $I_{LMAX}$  at  $V_{IN} = 6.0V$  for  $t = 10$  msec.  
**6:** Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value with a 1V differential applied.  
**7:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e.  $T_A, T_J, \theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum  $150^{\circ}C$  rating. Sustained junction temperatures above  $150^{\circ}C$  can impact the device reliability.  
**8:**  $V_{TH-MIN} = 2.55V$  and  $V_{TH-MAX} = 2.70V$ .  
**9:** The Junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

Unless otherwise specified, all limits are established for  $V_{IN} = V_R + 1$ ,  $I_L = 100 \mu A$ ,  $C_L = 3.3 \mu F$ ,  $\overline{SHDN} > V_{IH}$ ,  $T_A = 25^\circ C$ .  
**Boldface** type specifications apply for junction temperatures,  $T_J$  (**Note 9**) of  $-40^\circ C$  to  $+125^\circ C$ .

Parameter	Sym	Min	Typ	Max	Units	Conditions
VO <sub>UT</sub> Temperature Coefficient LDO1/LDO2/LDO3/LDO4	TCV <sub>OUT</sub>	—	20 <b>40</b>	—	ppm/°C	<b>Note 3</b>
Line Regulation LDO1/LDO2/ LDO3/LDO4	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	—	0.05	0.2	%/V	$(V_R + 1) \leq V_{IN} \leq 6.0V$
Load Regulation LDO1/LDO2/LDO3/LDO4	$\Delta V_{OUT}/V_{OUT}$	—	—	<b>2.0</b>	%	$I_L = 0.1 \text{ mA to } I_{OUT\_MAX}$ <b>Note 4</b>
Thermal Regulation LDO1/LDO2/LDO3/LDO4	$\Delta V_{OUT}/\Delta P_D$	—	0.04	—	V/W	<b>Note 5</b>
Dropout Voltage LDO1/LDO2/LDO3/LDO4	$V_{IN} - V_{OUT}$	—	2	—	mV	$I_L = 100 \mu A$ , <b>Note 6</b>
		—	15	—		$I_L = 20 \text{ mA}$ , <b>Note 6</b>
		—	35	<b>90</b>		$I_L = 50 \text{ mA}$ , <b>Note 6</b>
		—	100	<b>280</b>		$I_L = 150 \text{ mA}$ , <b>Note 6</b>
Output Noise LDO1/LDO2/LDO3/LDO4	$e_N$	—	1.2	—	$\mu V/(\text{Hz})^{1/2}$	$I_{OUT} = 100 \text{ mA}$ , $f = 10 \text{ kHz}$ $C_{OUT} = 1 \mu F$ to noise
<b>Over Temperature Protection Characteristics:</b>						
Thermal Shutdown Protection	T <sub>SD</sub>	—	150	—	°C	<b>Note 7</b>
Thermal Shutdown Hysteresis	$\Delta T_{SD}$	—	10	—	°C	
<b>SHDN Input Characteristics:</b>						
SHDN Input High Threshold	V <sub>IH</sub>	<b>60</b>	—	—	% of V <sub>IN</sub>	$V_{IN} = 2.7V$ to $6.0V$
SHDN Input Low Threshold	V <sub>IL</sub>	—	—	<b>15</b>	% of V <sub>IN</sub>	$V_{IN} = 2.7V$ to $6.0V$
Wake-up Time (from SHDN mode)	t <sub>WK</sub>	—	10	—	$\mu\text{sec}$	$V_{IN} = 5V$ , $I_L = 100 \text{ mA}$ , $C_{OUT} = 1 \mu F$ , $C_{IN} = 1 \mu F$ , see Figure 4-1
Settling Time (from SHDN mode)	t <sub>S</sub>	—	40	—	$\mu\text{sec}$	$V_{IN} = 5V$ , $I_L = 100 \text{ mA}$ , $C_{OUT} = 1 \mu F$ , $C_{IN} = 1 \mu F$ , See Figure 4-1
Shutdown Leakage Current	I <sub>SHDN</sub>	—	$\pm 0.01$	—	nA	$V_{SHDN} = V_{IN}$ or GND
<b>SELECT Input Characteristics:</b>						
SELECT Input High Threshold	V <sub>SELH</sub>	<b>V<sub>IN</sub>-0.2</b>	—	—	V	$V_{IN} = 2.7V$ to $6.0V$
SELECT Input Low Threshold	V <sub>SELL</sub>	—	—	<b>0.2</b>	V	$V_{IN} = 2.7V$ to $6.0V$
SELECT Input Leakage Current	I <sub>SELECT</sub>	—	$\pm 0.11$ $\pm 0.06$	—	$\mu A$	$V_{SELECT} = V_{IN}$ $V_{SELECT} = GND$
<b>RESET Output Characteristics:</b>						
Detect Operating Voltage Range	V <sub>DET</sub>	1.0 <b>1.2</b>	—	6.0 <b>6.0</b>	V	$T_A = 0^\circ C$ to $+70^\circ C$ $T_A = -40^\circ C$ to $+125^\circ C$

**Note 1:** The minimum  $V_{IN}$  must meet two conditions:  $V_{IN} \geq 2.7V$  and  $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$ .

**2:**  $V_R$  is the nominal regulator output voltage. For example:  $V_R = 1.8V, 2.5V, 2.8V$  or  $3.0V$ .

**3:**  $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta \text{Temperature})$ ,  $V_{OUT-HIGH}$  = Highest voltage measured over the temperature range.  $V_{OUT-LOW}$  = Lowest voltage measured over the temperature range.

**4:** Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1mA to the maximum specified output current. Changes in output voltage due to heating effects are determined using thermal regulation specification  $TCV_{OUT}$ .

**5:** Thermal regulation is defined as the change in output voltage at a time  $t$  after a change in power dissipation is applied. Specifications are for a current pulse equal to  $I_{LMAX}$  at  $V_{IN} = 6.0V$  for  $t = 10 \text{ msec}$ .

**6:** Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value with a 1V differential applied.

**7:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e.  $T_A, T_J, \theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum  $150^\circ C$  rating. Sustained junction temperatures above  $150^\circ C$  can impact the device reliability.

**8:**  $V_{TH-MIN} = 2.55V$  and  $V_{TH-MAX} = 2.70V$ .

**9:** The Junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

# TC1307

Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1$ , $I_L = 100 \mu A$ , $C_L = 3.3 \mu F$ , $\overline{SHDN} > V_{IH}$ , $T_A = 25^\circ C$ . <b>Boldface</b> type specifications apply for junction temperatures, $T_J$ ( <b>Note 9</b> ) of $-40^\circ C$ to $+125^\circ C$ .						
Parameter	Sym	Min	Typ	Max	Units	Conditions
Reset Threshold Voltage	$V_{TH}$	2.59 <b>2.55</b>	2.63 —	2.66 <b>2.70</b>	V V	$T_A = +25^\circ C$ $T_A = -40^\circ C$ to $+125^\circ C$ See Figure 4-2
Reset Circuit Supply Current	$I_{VDET}$	—	20	40	$\mu A$	$\overline{RESET} = \text{Open}$
Reset Threshold Voltage Temperature Coefficient	$V_{TH-TEMP}$	—	30	—	ppm/ $^\circ C$	
Detect Threshold to $\overline{RESET}$ Active Time Delay	$T_{VDET-RESET}$	—	135	—	$\mu sec$	$V_{DET} = V_{TH}$ to $V_{TH} - 100 mV$ , See Figure 4-2
Reset Time-out Period	$T_{RESET}$	<b>140</b>	300	<b>560</b>	msec	See Figure 4-2
$\overline{RESET}$ Output Voltage Low	$V_{OL-RES}$	—	—	<b>0.3</b>	V	$V_{DET} = V_{TH-min}$ $I_{SINK} = 1.2 mA$
		—	—	<b>0.4</b>		$V_{DET} = V_{TH-min}$ $I_{SINK} = 3.2 mA$
		—	—	<b>0.3</b>		$V_{DET} > 1.0V$ $I_{SINK} = 50 \mu A$ <b>Note 8</b> , See Figure 4-2
$\overline{RESET}$ Output Voltage High	$V_{OH-RES}$	$0.8 * V_{DET}$ $V_{DET} = 1.5V$	—	—	V	$I_{SOURCE} = 500 \mu A$ $I_{SOURCE} = 800 \mu A$ $V_{DET} > V_{TH-max}$ (Both cases), See Figure 4-2
<b>Temperature Ranges:</b>						
Maximum Junction Temperature Range	$T_J$	-40	—	+150	$^\circ C$	
Maximum Junction Temperature Range	$T_J$	-40	—	+125	$^\circ C$	
Storage Temperature Range	$T_A$	-65	—	+150	$^\circ C$	
<b>Thermal Package Resistances:</b>						
Thermal Resistance, 16L-QSOP	$\theta_{JA}$	—	112.4	—	$^\circ C/W$	EIA/JEDEC JESD51-751-7 4 Layer Board

- Note 1:** The minimum  $V_{IN}$  must meet two conditions:  $V_{IN} \geq 2.7V$  and  $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$ .
- 2:**  $V_R$  is the nominal regulator output voltage. For example:  $V_R = 1.8V, 2.5V, 2.8V$  or  $3.0V$ .
- 3:**  $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$ .  $V_{OUT-HIGH}$  = Highest voltage measured over the temperature range.  $V_{OUT-LOW}$  = Lowest voltage measured over the temperature range.
- 4:** Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1mA to the maximum specified output current. Changes in output voltage due to heating effects are determined using thermal regulation specification  $TCV_{OUT}$ .
- 5:** Thermal regulation is defined as the change in output voltage at a time  $t$  after a change in power dissipation is applied. Specifications are for a current pulse equal to  $I_{LMAX}$  at  $V_{IN} = 6.0V$  for  $t = 10 msec$ .
- 6:** Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value with a 1V differential applied.
- 7:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e.  $T_A, T_J, \theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum  $150^\circ C$  rating. Sustained junction temperatures above  $150^\circ C$  can impact the device reliability.
- 8:**  $V_{TH-MIN} = 2.55V$  and  $V_{TH-MAX} = 2.70V$ .
- 9:** The Junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

## 2.0 TYPICAL PERFORMANCE CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated,  $V_{IN} = 3.8V$ ,  $C_{IN} = 10 \mu F$  ceramic (X5R),  $C_{OUT} = 1 \mu F$  ceramic (X5R),  $I_{LOAD} = 100 \mu A$ , SELECT12 = NC, SELECT34 =  $V_{IN}$ , SHDN1/2/3/4 =  $V_{IN}$ ,  $T_A = 25^\circ C$ .

Junction temperature ( $T_J$ ) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

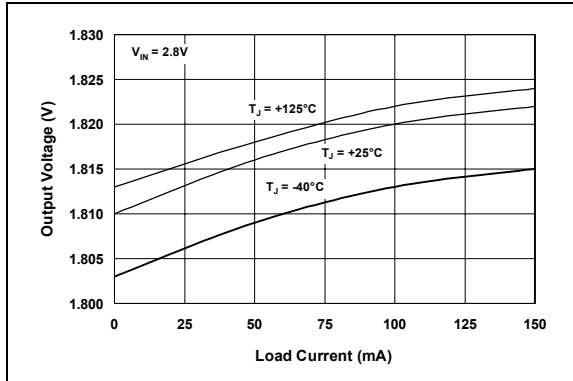


FIGURE 2-1:  $V_{OUT}$  vs. Load Current.

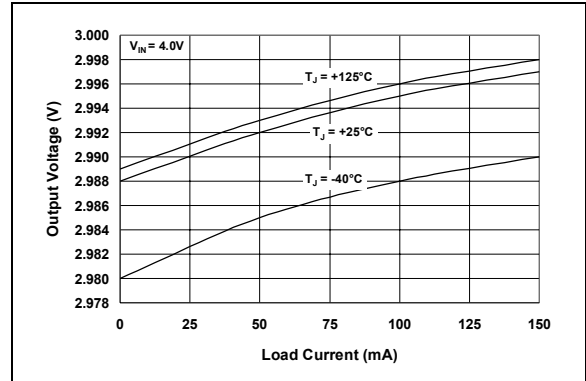


FIGURE 2-4:  $V_{OUT}$  vs. Load Current.

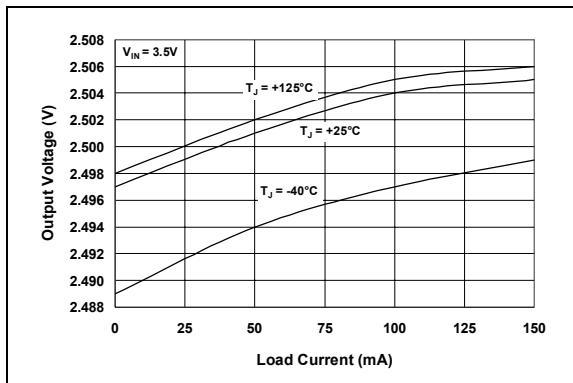


FIGURE 2-2:  $V_{OUT}$  vs. Load Current.

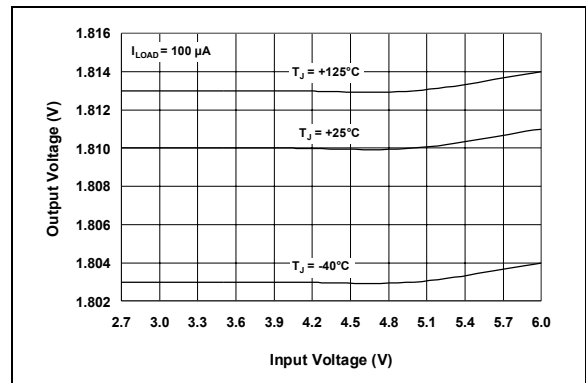


FIGURE 2-5:  $V_{OUT}$  vs. Input Voltage.

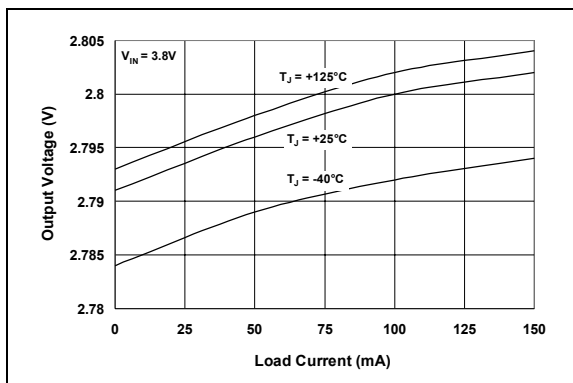


FIGURE 2-3:  $V_{OUT}$  vs. Load Current.

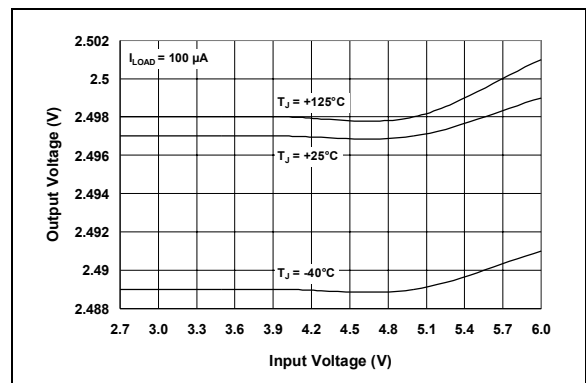
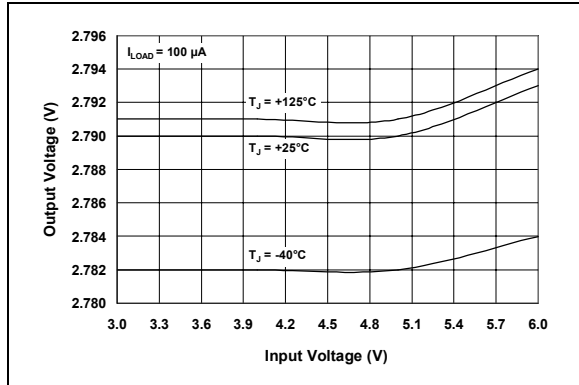


FIGURE 2-6:  $V_{OUT}$  vs. Input Voltage.

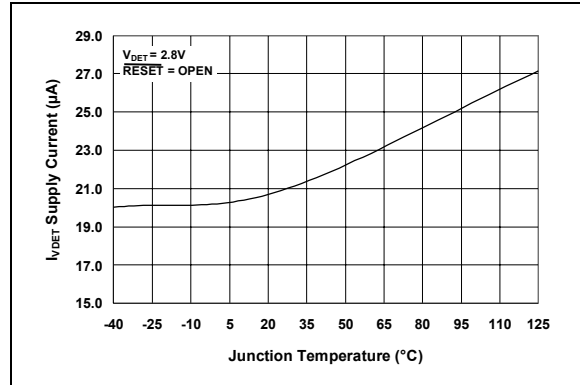
# TC1307

**Note:** Unless otherwise indicated,  $V_{IN} = 3.8V$ ,  $C_{IN} = 10 \mu F$  ceramic (X5R),  $C_{OUT} = 1 \mu F$  ceramic (X5R),  $I_{LOAD} = 100 \mu A$ ,  $SELECT12 = NC$ ,  $SELECT34 = V_{IN}$ ,  $SHDN1/2/3/4 = V_{IN}$ ,  $T_A = 25^\circ C$ .

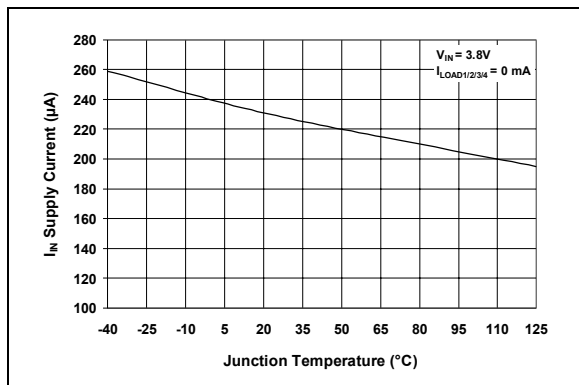
Junction temperature ( $T_J$ ) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.



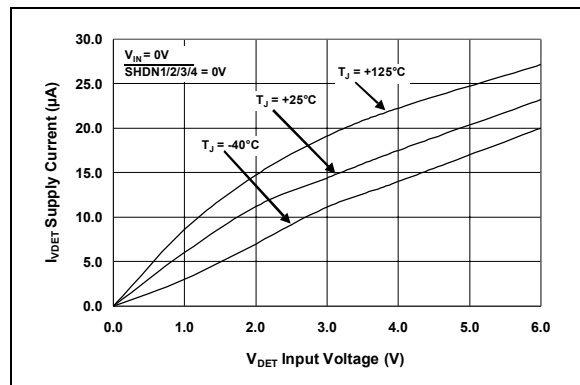
**FIGURE 2-7:**  $V_{OUT}$  vs. Input Voltage.



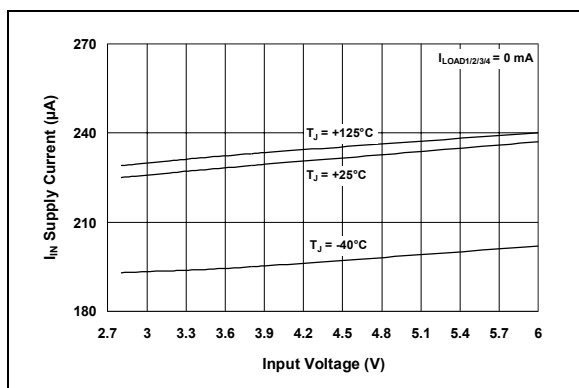
**FIGURE 2-10:**  $V_{DET}$  Supply Current vs. Junction Temperature.



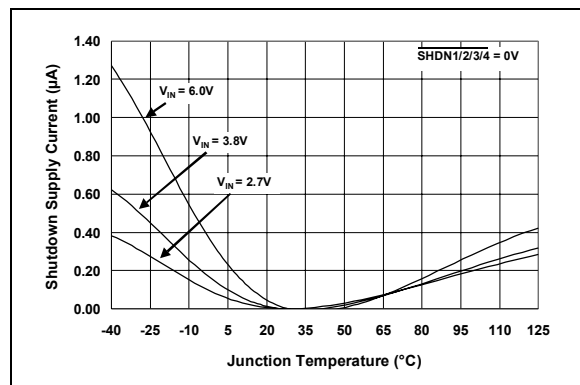
**FIGURE 2-8:**  $V_{IN}$  Supply Current vs. Junction Temperature.



**FIGURE 2-11:**  $V_{DET}$  Supply Current vs.  $V_{DET}$  Input Voltage.



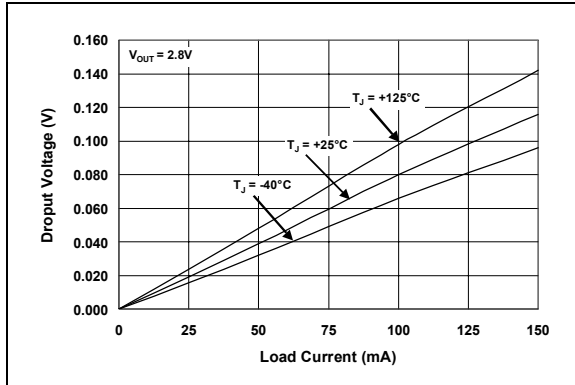
**FIGURE 2-9:** Supply Current vs. Input Voltage,  $V_{IN}$ .



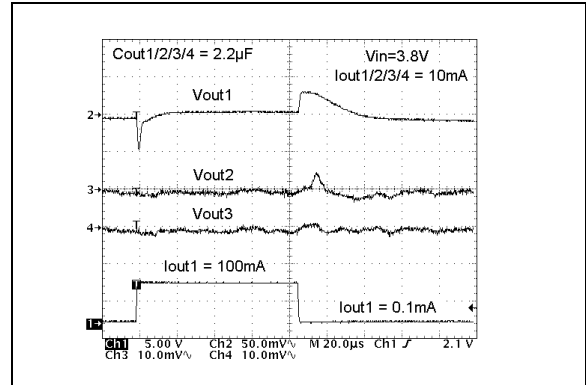
**FIGURE 2-12:** Supply Current vs. Junction Temperature.

**Note:** Unless otherwise indicated,  $V_{IN} = 3.8V$ ,  $C_{IN} = 10 \mu F$  ceramic (X5R),  $C_{OUT} = 1 \mu F$  ceramic (X5R),  $I_{LOAD} = 100 \mu A$ ,  $SELECT12 = NC$ ,  $SELECT34 = V_{IN}$ ,  $SHDN1/2/3/4 = V_{IN}$ ,  $T_A = 25^\circ C$ .

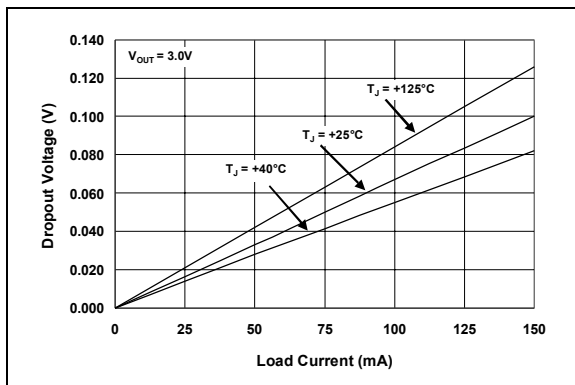
Junction temperature ( $T_J$ ) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.



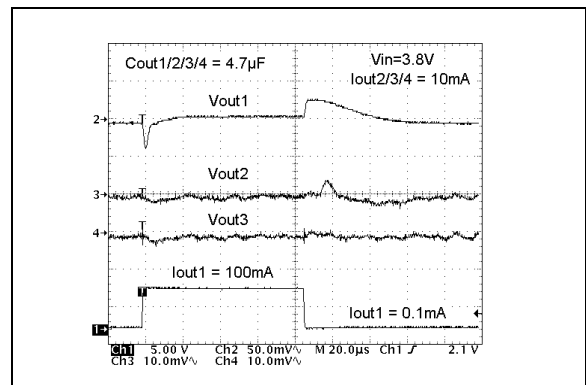
**FIGURE 2-13:** Dropout Voltage vs. Load Current.



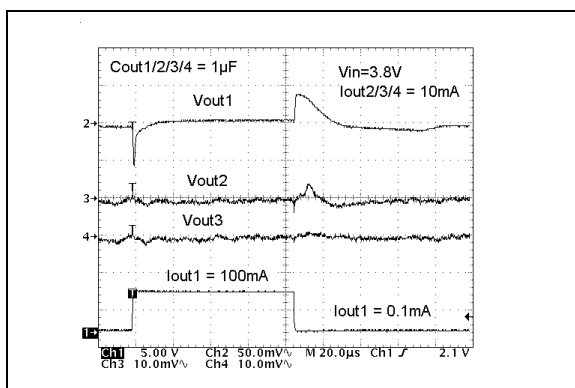
**FIGURE 2-16:** Crosstalk Characteristics  $V_{OUT1}$ ,  $V_{OUT2}$ , and  $V_{OUT3}$ .



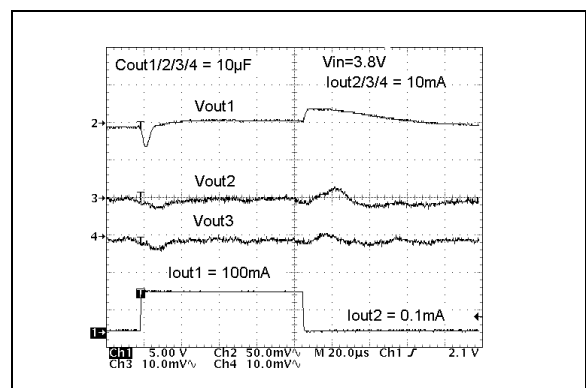
**FIGURE 2-14:** Dropout Voltage vs. Load Current.



**FIGURE 2-17:** Crosstalk Characteristics  $V_{OUT1}$ ,  $V_{OUT2}$ , and  $V_{OUT3}$ .



**FIGURE 2-15:** Crosstalk Characteristics  $V_{OUT1}$ ,  $V_{OUT2}$  and  $V_{OUT3}$ .

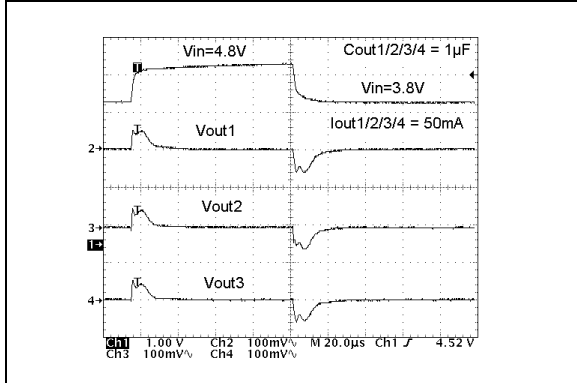


**FIGURE 2-18:** Crosstalk Characteristics  $V_{OUT1}$ ,  $V_{OUT2}$ , and  $V_{OUT3}$ .

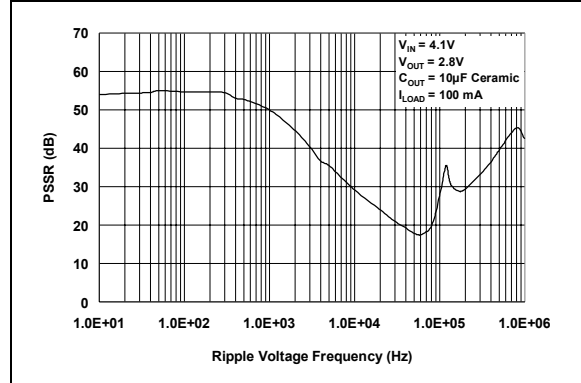
# TC1307

**Note:** Unless otherwise indicated,  $V_{IN} = 3.8V$ ,  $C_{IN} = 10 \mu F$  ceramic (X5R),  $C_{OUT} = 1 \mu F$  ceramic (X5R),  $I_{LOAD} = 100 \mu A$ , SELECT12 = NC, SELECT34 =  $V_{IN}$ , SHDN1/2/3/4 =  $V_{IN}$ ,  $T_A = 25^\circ C$ .

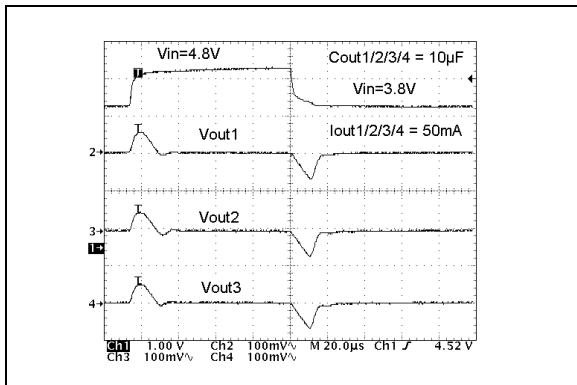
Junction temperature ( $T_J$ ) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.



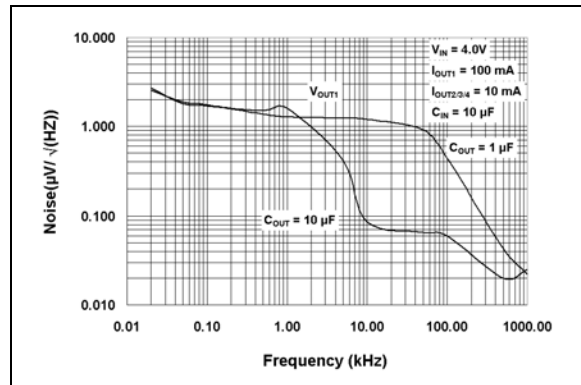
**FIGURE 2-19:** Line Step Response.



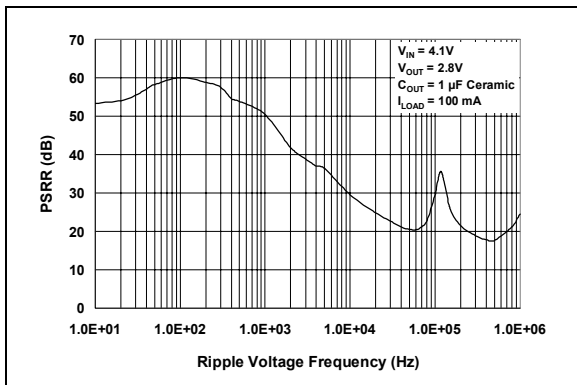
**FIGURE 2-22:** Power Supply Rejection Ratio vs. Ripple Voltage Frequency.



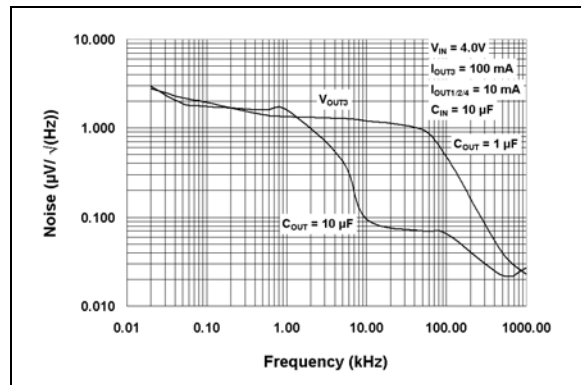
**FIGURE 2-20:** Line Step Response.



**FIGURE 2-23:** Output Noise.



**FIGURE 2-21:** Power Supply Rejection Ratio vs. Ripple Voltage Frequency.

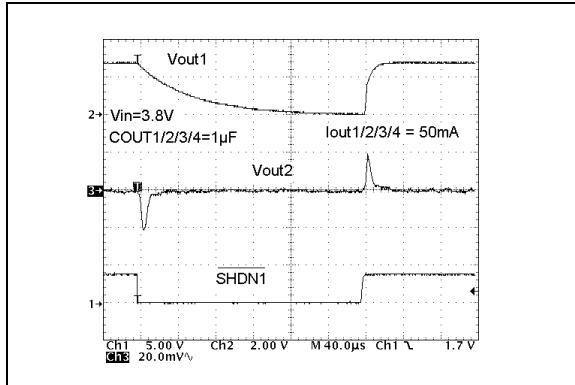


**FIGURE 2-24:** Output Noise.

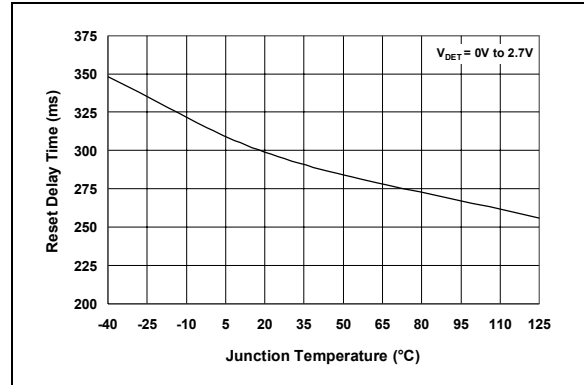


**Note:** Unless otherwise indicated,  $V_{IN} = 3.8V$ ,  $C_{IN} = 10 \mu F$  ceramic (X5R),  $C_{OUT} = 1 \mu F$  ceramic (X5R),  $I_{LOAD} = 100 \mu A$ ,  $SELECT12 = NC$ ,  $SELECT34 = V_{IN}$ ,  $SHDN1/2/3/4 = V_{IN}$ ,  $T_A = 25^\circ C$ .

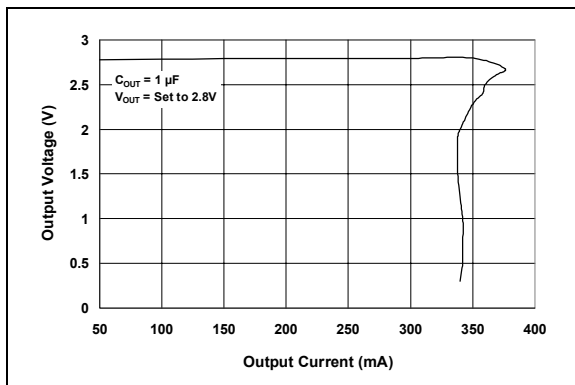
Junction temperature ( $T_J$ ) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.



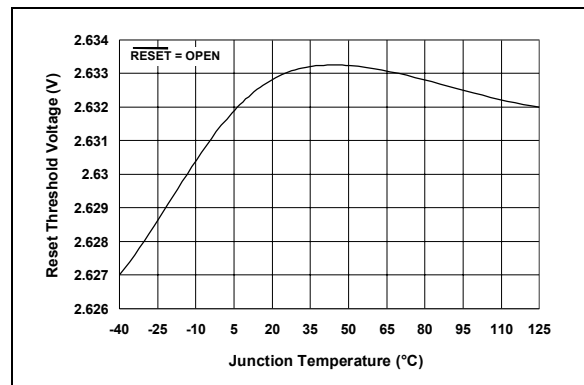
**FIGURE 2-25:** Response From SHDN1.



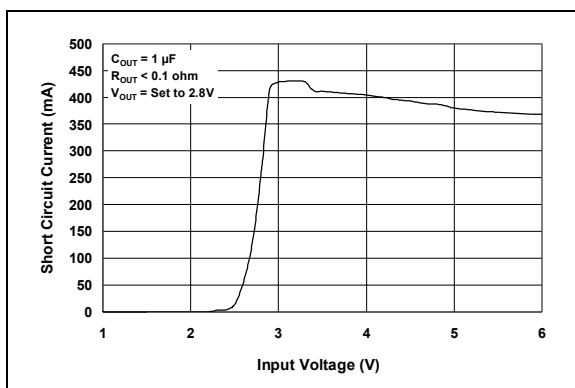
**FIGURE 2-28:** Power-Up Reset Time-out Period vs. Junction Temperature.



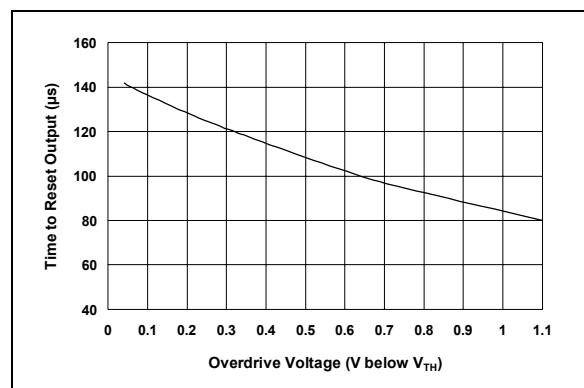
**FIGURE 2-26:** Output Voltage vs. Current.



**FIGURE 2-29:** Reset Threshold Voltage vs. Junction Temperature.



**FIGURE 2-27:** Short Circuit Current vs. Input Voltage.

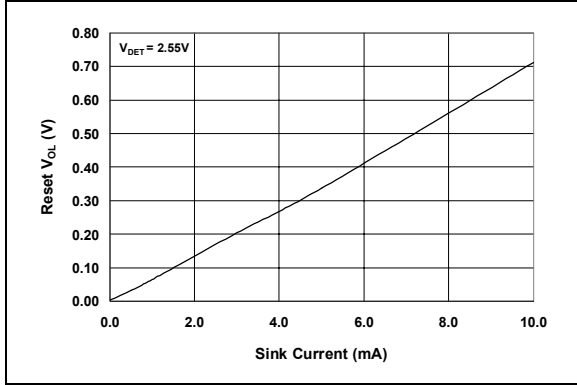


**FIGURE 2-30:** Reset Delay vs. Overdrive Voltage.

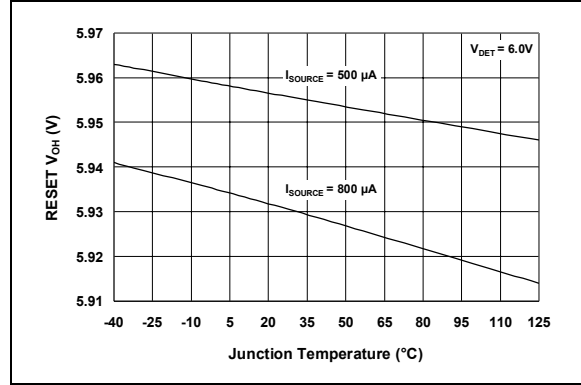
# TC1307

**Note:** Unless otherwise indicated,  $V_{IN} = 3.8V$ ,  $C_{IN} = 10 \mu F$  ceramic (X5R),  $C_{OUT} = 1 \mu F$  ceramic (X5R),  $I_{LOAD} = 100 \mu A$ ,  $SELECT12 = NC$ ,  $SELECT34 = V_{IN}$ ,  $SHDN1/2/3/4 = V_{IN}$ ,  $T_A = 25^\circ C$ .

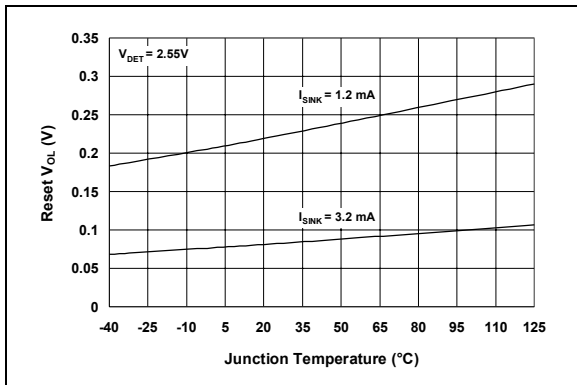
Junction temperature ( $T_J$ ) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.



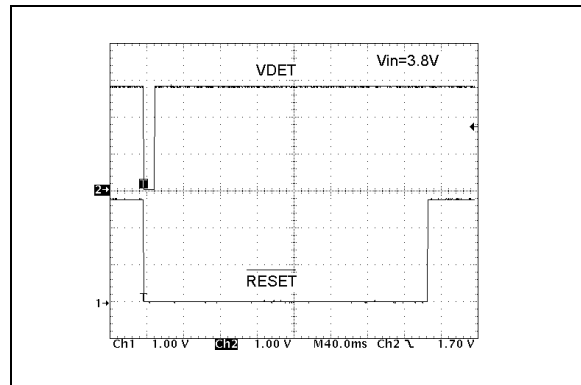
**FIGURE 2-31:** Reset  $V_{OL-RES}$  vs.  $I_{SINK}$ .



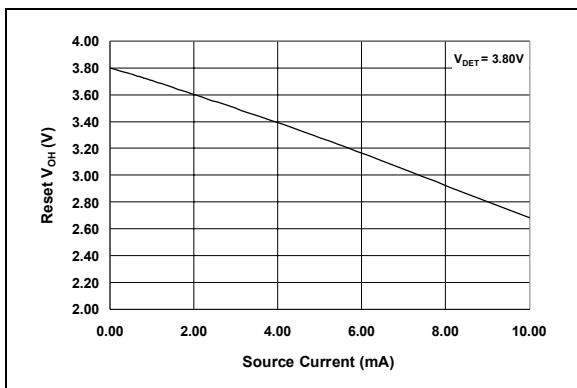
**FIGURE 2-34:** Reset  $V_{OH-RES}$  vs. Junction Temperature.



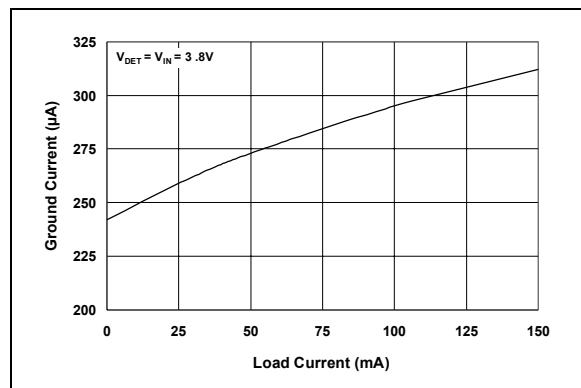
**FIGURE 2-32:** Reset  $V_{OL-RES}$  vs. Junction Temperature.



**FIGURE 2-35:** Power-Up  $\overline{RESET}$  Timing.



**FIGURE 2-33:** Reset  $V_{OH-RES}$  vs.  $I_{SOURCE}$ .



**FIGURE 2-36:** Ground Current vs. Load Current.

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

Name	Function
V <sub>DET</sub>	Voltage Detect Input
SHDN1	Shutdown for V <sub>OUT1</sub>
SELECT12	Input for setting V <sub>OUT1</sub> and V <sub>OUT2</sub> .
V <sub>IN</sub>	Input Voltage Connection
V <sub>IN</sub>	Input Voltage Connection
GND	Ground connection
SHDN3	Shutdown for V <sub>OUT3</sub>
V <sub>IN</sub>	Input Voltage Connection
SHDN4	Shutdown for V <sub>OUT4</sub>
SELECT34	Input for setting V <sub>OUT3</sub> and V <sub>OUT4</sub> .
V <sub>OUT4</sub>	LDO4 Output
V <sub>OUT3</sub>	LDO3 Output
V <sub>OUT2</sub>	LDO2 Output
V <sub>OUT1</sub>	LDO1 Output
SHDN2	Shutdown for V <sub>OUT2</sub>
RESET	Reset Output

**TABLE 3-1:** Pin Description Table.

### 3.1 Voltage Detect Input (V<sub>DET</sub>)

Input pin that is compared to internal threshold voltage (typically 2.63V). When the V<sub>DET</sub> input is below the 2.63V threshold, the RESET output is held in its normal low state. When the input voltage on the V<sub>DET</sub> pin rises above the threshold voltage, the RESET output pin remains low for 300 mS (Typical). After the delay, the RESET pin changes to a logic high state.

### 3.2 Shutdown Control Input for V<sub>OUT1</sub> (SHDN1)

LDO#1 output is enabled when a logic high is applied to the SHDN1 input. LDO#1 output is disabled with a logic low tied to the SHDN1 pin. When shutdown, LDO#1 enters a low quiescent current state and the linear pass P-Channel MOSFET is off. The RESET output remains valid and is independent of SHDN1.

### 3.3 SELECT Control Input for Setting V<sub>OUT1</sub> and V<sub>OUT2</sub> (SELECT12)

Input pin used to select the output voltage of LDO#1 and LDO#2. When SELECT is tied to V<sub>IN</sub>, V<sub>OUT1</sub> = V<sub>OUT2</sub> = 3.0V. When SELECT is tied to GND, V<sub>OUT1</sub> = V<sub>OUT2</sub> = 2.5V. If the SELECT input is not connected, V<sub>OUT1</sub> = V<sub>OUT2</sub> = 2.8V.

### 3.4 Input Voltage V<sub>IN</sub>

Connect input source to this pin. All V<sub>IN</sub> pins must be tied together.

### 3.5 Ground (GND)

Connect this pin to the circuit ground. NOTE: This pin does not carry high current and should be connected to quiet circuit ground.

### 3.6 Shutdown Control Input for V<sub>OUT3</sub> (SHDN3)

LDO#3 output is enabled when a logic high is applied to the SHDN3 input. LDO#3 output is disabled with a logic low tied to the SHDN3 pin. When shutdown, LDO#3 enters a low quiescent current state and the linear pass P-Channel MOSFET is off. The RESET output remains valid and is independent of SHDN3.

### 3.7 Shutdown Control Input for V<sub>OUT4</sub> (SHDN4)

LDO#4 output is enabled when a logic high is applied to the SHDN4 input. LDO#4 output is disabled with a logic low tied to the SHDN4 pin. When shutdown, LDO#4 enters a low quiescent current state and the linear pass P-Channel MOSFET is off. The RESET output remains valid and is independent of SHDN4.

### 3.8 SELECT Control Input for Setting V<sub>OUT3</sub> and V<sub>OUT4</sub> (SELECT34)

Input pin used to select the output voltage of LDO#3 and LDO#4. When SELECT is tied to V<sub>IN</sub>, V<sub>OUT3</sub> = V<sub>OUT4</sub> = 2.8V. When SELECT is tied to GND, V<sub>OUT3</sub> = V<sub>OUT4</sub> = 1.8V. If the SELECT input is not connected, V<sub>OUT3</sub> = V<sub>OUT4</sub> = 2.5V.

### 3.9 Regulated Output Voltage #4 (V<sub>OUT4</sub>)

Output voltage selected by tri-state input SELECT34. Output can be set to 1.80V, 2.50V or 2.80V

### 3.10 Regulated Output Voltage #3 (V<sub>OUT3</sub>)

Output voltage selected by tri-state input SELECT34. Output can be set to 1.80V, 2.50V or 2.80V

### 3.11 Regulated Output Voltage #2 (V<sub>OUT2</sub>)

Output voltage selected by tri-state input SELECT12. Output can be set to 2.50V, 2.80V or 3.00V

### 3.12 Regulated Output Voltage #1 (V<sub>OUT1</sub>)

Output voltage selected by tri-state input SELECT12. Output can be set to 2.50V, 2.80V or 3.00V.

### 3.13 Shutdown Control Input for V<sub>OUT2</sub> (SHDN2)

LDO#2 output is enabled when a logic high is applied to the SHDN2 input. LDO#2 output is disabled with a logic low tied to the SHDN2 pin. When shutdown, LDO#2 enters a low quiescent current state and the linear pass P-Channel MOSFET is off. The  $\overline{\text{RESET}}$  output remains valid and is independent of SHDN2.

### 3.14 RESET Output ( $\overline{\text{RESET}}$ )

Logic low output when voltage on V<sub>DET</sub> pin is below the RESET Threshold Voltage. When the voltage on the V<sub>DET</sub> pin rises above the RESET Threshold Voltage, the RESET output will remain low for the RESET Time-out Period and then transition to a logic high.

## 4.0 DEVICE OVERVIEW

The TC1307 integrates four high performance linear Low Dropout Regulators and a microcontroller reset function.

As shown in the block diagram (Figure 4-3) using dashed lines, each LDO has an independent shutdown, error amplifier, P-MOS pass transistor and feedback divider resistors. All four LDOs share a common voltage reference. LDO output numbers one and two share a tri-state select input while LDO numbers three and four share a tri-state select input. The select input is used to program the LDO output voltage.

Also shown in the block diagram is the microcontroller reset monitor. The reset monitor voltage detect input is independent of the LDO input or output voltages.

### 4.1 Low Dropout Out Linear Regulators

#### 4.1.1 OUTPUT

The TC1307 integrates four low drop out linear regulators. Each regulator has 150 mA output current capability. A minimum of 1  $\mu\text{F}$  output capacitance is required on each of the LDOs for circuit stability. The output capacitor type can be ceramic, tantalum or aluminum. The esr range required for the output capacitor is 0  $\Omega$  to 2  $\Omega$ . To improve the dynamic performance of the LDO in cases where sudden input voltage changes or load current changes are present, larger capacitors can be used.

The output voltage of the LDO can be selected using the SELECT input pins. Table 4-1 summarizes how to select the desired LDO output voltage for  $V_{\text{OUT1}}$  and  $V_{\text{OUT2}}$ . Table 4-2 summarizes how to select the desired LDO output voltage for  $V_{\text{OUT3}}$  and  $V_{\text{OUT4}}$ .

SELECT12	$V_{\text{OUT1}}$	$V_{\text{OUT2}}$
GND	2.50V	2.50V
No Connect	2.80V	2.80V
$V_{\text{IN}}$	3.00V	3.00V

**TABLE 4-1:** SELECT12 MODE settings.

SELECT34	$V_{\text{OUT3}}$	$V_{\text{OUT4}}$
GND	1.80V	1.80V
No Connect	2.50V	2.50V
$V_{\text{IN}}$	2.80V	2.80V

**TABLE 4-2:** SELECT34 MODE Settings.

#### 4.1.2 INPUT

The TC1307, like all low drop out linear regulators, requires a relatively low source impedance ( $< 10 \Omega$ ) tied to the  $V_{\text{IN}}$  pin of the device to ensure circuit stability. For battery applications or in applications that have long lead length from the input voltage source to the LDO  $V_{\text{IN}}$  pin, a minimum capacitance of 2.2  $\mu\text{F}$  is rec-

ommended to lower the source impedance. For applications that have more than 1  $\mu\text{F}$  of capacitance on the LDO outputs, higher input capacitance (4.7  $\mu\text{F}$ ) may be needed to ensure stability.

#### 4.1.3 SHUTDOWN OPERATION

Each LDO output can be enabled and disabled using its respective shutdown input pin. For example, when the level on  $\overline{\text{SHDN1}}$  is below the logic low level threshold ( $V_{\text{IL}}$ ), LDO#1 output is disabled (P-Channel MOSFET is turned OFF). If all four shutdown inputs are below  $V_{\text{IL}}$ , the bandgap reference is turned off and the shutdown current is typically less than 0.1  $\mu\text{A}$ . The LDO output will typically wake-up in 10  $\mu\text{s}$  and the output will settle in approximately 40  $\mu\text{s}$  when brought out of shutdown mode. See Figure 4-1 for timing definition. The microcontroller RESET output function is independent of all SHDN input pins.

### 4.2 Voltage Reset Monitor

The independent voltage reset output of the TC1307 can be used for low battery input voltage detect or microcontroller power on reset function. The voltage reset function monitors the voltage on the  $V_{\text{DET}}$  pin. The active low  $\overline{\text{RESET}}$  output is capable of sourcing and sinking current (Push-Pull). When the voltage on the  $V_{\text{DET}}$  pin is below the 2.63V typical threshold, the RESET output pin is active low and capable of sinking 3.2 mA while holding the RESET output voltage below 0.4V. When the voltage on the  $V_{\text{DET}}$  pin rises above the 2.63V typical threshold, the  $\overline{\text{RESET}}$  output will remain low for the  $T_{\overline{\text{RESET}}}$  time period. After the  $\overline{\text{RESET}}$  time out period, the RESET output voltage will transition to the high output state ( $> V_{\text{DET}} - 1.5\text{V}$  when sourcing 800  $\mu\text{A}$ ), if the  $V_{\text{DET}}$  pin remains above the threshold voltage. The RESET output is current limited. The maximum source or sink current recommended for normal operation is 10 mA.

The  $\overline{\text{RESET}}$  output will be driven low within 100  $\mu\text{sec}$  of  $V_{\text{DET}}$  pin going below the  $\overline{\text{RESET}}$  voltage threshold of 2.63V typical. The  $\overline{\text{RESET}}$  output will remain valid for  $V_{\text{DET}}$  voltages greater than 1.0V. See Figure 4-2 for  $V_{\text{DET}}$  and RESET output timing diagram.

# TC1307

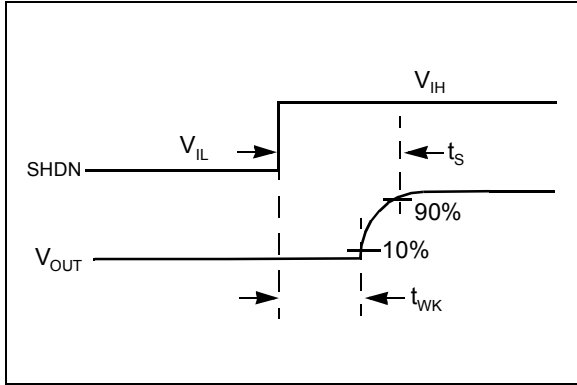


FIGURE 4-1: Wake-up From SHDN.

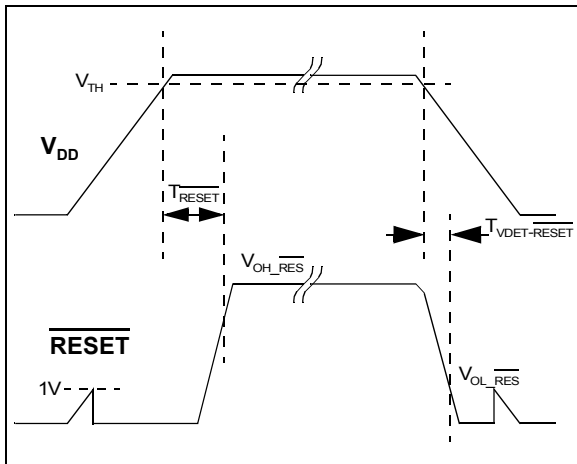
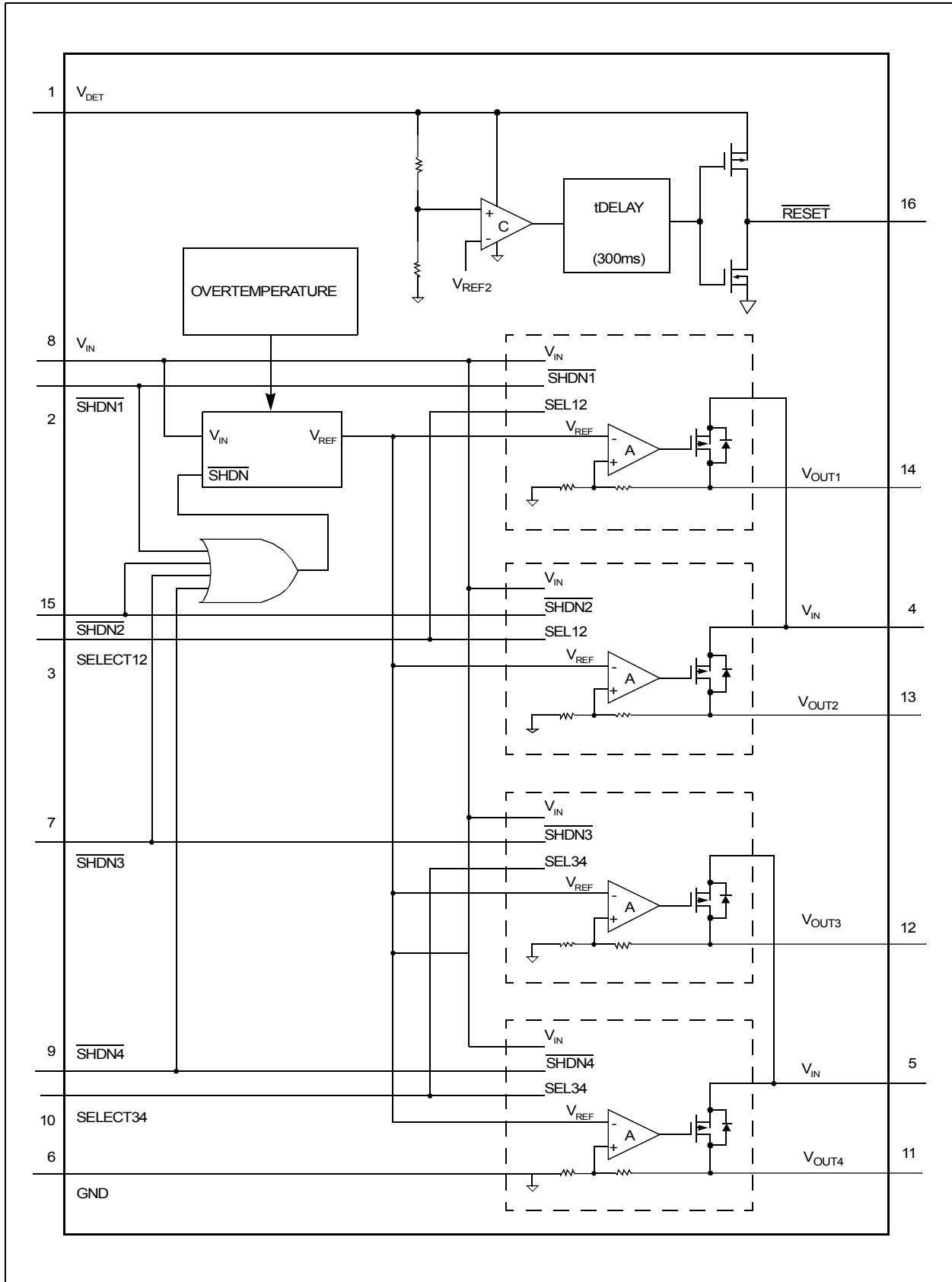


FIGURE 4-2: RESET Timing Diagram.



**FIGURE 4-3:** TC1307 Block Diagram.

# TC1307

## 5.0 APPLICATIONS

### 5.1 Load Partitioning

The TC1307 can be used to power two separate channels for a wide range of applications. Each channel can be turned ON and OFF independently of the other. In this example, the SELECT12 pin is tied to  $V_{IN}$  and the SELECT34 pin is tied to GND. The output voltages of  $V_{OUT1}$  and  $V_{OUT2}$  are 3.0V and the output voltage of  $V_{OUT3}$  and  $V_{OUT4}$  are 1.8V. If  $V_{OUT1}$  and  $V_{OUT3}$  were powering 1 Channel and  $V_{OUT2}$  and  $V_{OUT4}$  were powering an identical Channel, either Channel could be powered independent of the other Channel. The output voltage of  $V_{OUT1}$  is being monitored by the internal voltage detection circuit. When the output of  $V_{OUT1}$  is below the typical 2.63V threshold voltage, the RESET output will transition low.

### 5.2 Input Capacitor

Low input source impedance is necessary for the LDO to operate properly. When operating off of batteries or in applications with long lead length (>10") between the input source and the LDO, some input capacitance is required. A minimum of 2.2  $\mu\text{F}$  is recommended for most applications and the capacitor should be placed as close to the input of the LDO as practical (>0.2"). Larger input capacitors will help reduce the input impedance and further reduce any high frequency noise on the input and output of the LDO. If more than 1  $\mu\text{F}$  of capacitance is used on the LDO outputs, a 4.7  $\mu\text{F}$  input capacitor is recommended.

### 5.3 Output Capacitor

A minimum output capacitance of 1  $\mu\text{F}$  for the TC1307 is required for stability. The esr requirements on the output capacitor are between 0 and 2 ohms. The output capacitor should be located as close to the LDO output as practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable esr range required. A typical 1  $\mu\text{F}$  X5R 0805 capacitor has an esr of 50 milli-ohms. Larger output capacitors can be used with the TC1307 to improve dynamic behavior, noise and ripple rejection performance.

### 5.4 Power Dissipation

The internal power loading within the TC1307 is a function of input voltage, output voltage, output current, quiescent current and RESET output dissipation. For many applications the power dissipation within the linear P-Channel device can be used as a good approximation of total power dissipation. This is due to the low quiescent current consumed even when the LDO output is providing full load current (150 mA).

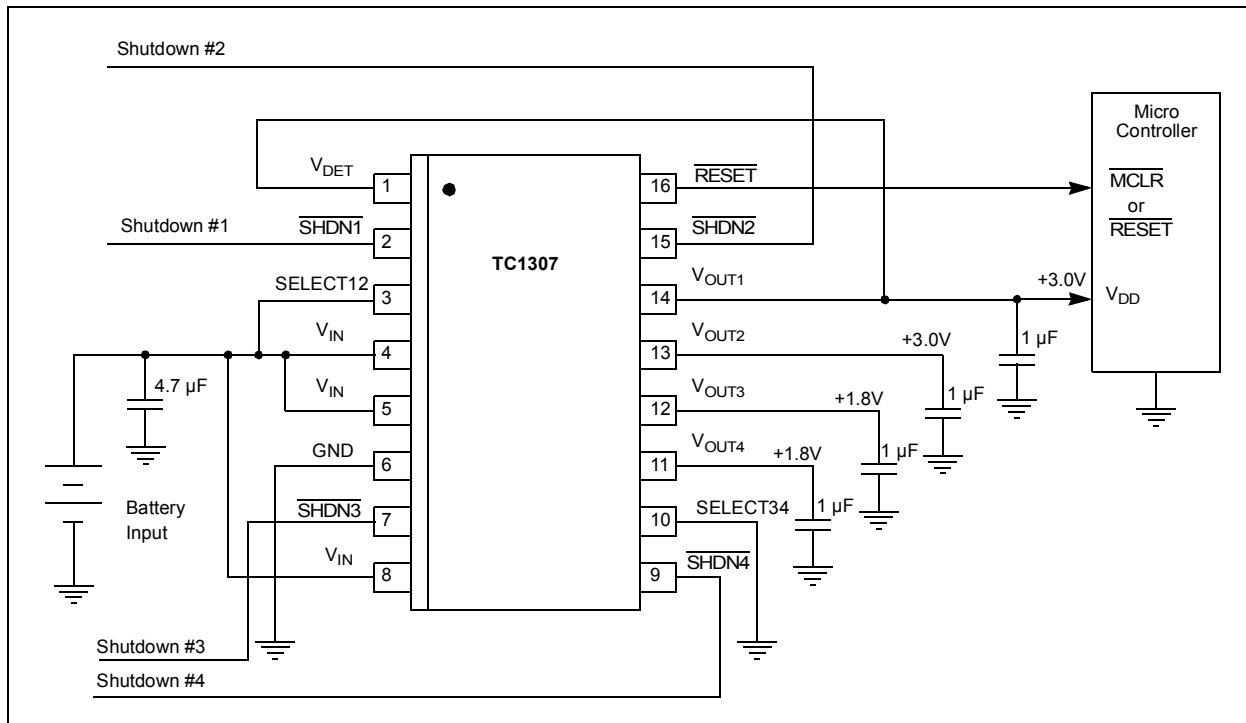


FIGURE 5-1: Typical 4 Output with RESET Application.



## 5.4.1 P-CHANNEL LINEAR PASS DEVICE

$$P_{Linear} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

Where:

$P_{Linear}$  = Power dissipated in the LDO P-Channel linear pass element.

$V_{IN(MAX)}$  = Maximum input voltage ( $V_{IN}$ )

$V_{OUT(MIN)}$  = Minimum LDO output Voltage ( $V_{OUT}$ )

$I_{OUT(MAX)}$  = Maximum LDO output current

## 5.4.2 QUIESCENT CURRENT

The quiescent current consumed by the TC1307 has two components. The quiescent current required to bias the LDO regulators and the quiescent current required to bias the voltage detection circuitry. To determine the power dissipation as a result of the total device quiescent current both the maximum input voltage on the  $V_{IN}$  and  $V_{DET}$  inputs should be used.

$$P_Q = V_{IN} \times I_{IN} + V_{DET} \times I_{DET}$$

Where:

$P_Q$  = Power internal to the LDO as a result of internal biasing

$V_{IN}$  = Input voltage

$I_{IN}$  = Input current when all load currents = 0 mA

$V_{DET}$  = Detect Input Voltage

$I_{VDET}$  = Voltage detect input pin current

## 5.4.3 $\overline{RESET}$ OUTPUT

The power dissipation for the  $\overline{RESET}$  output driver can be a result of the sinking current or sourcing current depending on the state of the output.

$$P_{RESET} = V_{OL} \times I_{SINK}$$

Where:

$P_{RESET}$  = Power dissipated as a result of the  $\overline{RESET}$  output.

$V_{OL}$  =  $\overline{RESET}$  low output voltage

$I_{SINK}$  =  $\overline{RESET}$  sink current

The power dissipation internal to the  $\overline{RESET}$  output due to sourcing current can be calculated by using the following equation.

$$P_{RESET} = (V_{DET} - V_{SOURCE}) \times I_{SOURCE}$$

Where:

$P_{RESET}$  = Power dissipation as a result of  $\overline{RESET}$  output while in the high state

$V_{DET}$  = Detect Voltage

$V_{SOURCE}$  =  $\overline{RESET}$  output pin voltage while in the high state

$I_{SOURCE}$  = Output current being sourced

## 5.4.4 TOTAL INTERNAL POWER DISSIPATION

The total power dissipated within the TC1307 is the sum of the power dissipated in each of the four LDOs, the  $P_Q$  term and the  $P_{RESET}$  term (either sinking or sourcing). Because of the CMOS construction, the typical  $I_{IN}$  for the TC1307 is 220  $\mu$ A. When operating at a maximum of 5V this results in a power dissipation of 1.2 milli-Watts. For most applications this is small compared to the LDO pass device power dissipation and can be neglected. The  $P_{RESET}$  term for a typical 3.2 mA sinking application will dissipate a maximum of 3.2 mA x 0.4V or 1.28 milli-Watts. A typical sourcing application of 800  $\mu$ A will have a maximum 1.5V drop from the  $V_{DET}$  voltage will dissipate a maximum of 800  $\mu$ A x 1.5V or 1.2 milli-Watts. Again for most applications this is small compared to the LDO pass device power dissipation and can be neglected.

$$P_{TOTAL} = P_{Linear} + P_Q + P_{RESET}$$

## 5.4.5 MAXIMUM JUNCTION TEMPERATURE

The operating junction temperature ( $T_J$ ) specified for the TC1307 is 125°C. To estimate the internal junction temperature of the TC1307, the total internal power dissipation ( $P_{TOTAL}$ ) is multiplied by the thermal resistance from junction to ambient ( $\theta_{JA}$ ) of the device. The thermal resistance from junction to ambient for the QSOP 16-pin package is estimated at 112.4°C/W. The actual thermal resistance from junction to air can vary from application to application for the QSOP16 depending on board copper area, copper thickness, airflow and other external environmental factors.

$$T_{J(MAX)} = P_{TOTAL} \times \theta_{JA}$$

The maximum power dissipation capability for a package ( $P_{D(MAX)}$ ) can be calculated given the junction to air thermal resistance and the maximum ambient temperature ( $T_{A(MAX)}$ ) for the application. The following equation can be used to determine the package maximum internal power dissipation.

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{\theta_{JA}}$$

## 5.5 Typical Application

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation as a result of quiescent current and RESET output are small enough to be neglected.

### Input Voltage:

$$V_{IN} = 3.1V \text{ to } 4.1V$$

### LDO Output Voltages and Currents:

$$V_{OUT1} = 3.0V$$

$$I_{IOUT1} = 100 \text{ mA}$$

$$V_{OUT2} = 3.0V$$

$$I_{IOUT2} = 100 \text{ mA}$$

$$V_{OUT3} = 1.8V$$

$$I_{IOUT3} = 60 \text{ mA}$$

$$V_{OUT4} = 1.8V$$

$$I_{IOUT4} = 60 \text{ mA}$$

### Maximum Ambient Temperature:

$$T_{A(MAX)} = 50^{\circ}\text{C}$$

### Internal Power Dissipation:

Internal Power dissipation is the sum of the power dissipation for each LDO pass device.

$$P_{LDO1} = (V_{IN(MAX)} - V_{OUT1(MIN)}) \times I_{OUT1(MAX)}$$

$$P_{LDO1} = (4.1V - (0.975 \times 3.0V)) \times 100 \text{ mA}$$

$$P_{LDO1} = 117.5 \text{ milli-Watts}$$

$$P_{LDO2} = (4.1V - (0.975 \times 3.0V)) \times 100 \text{ mA}$$

$$P_{LDO2} = 117.5 \text{ milli-Watts}$$

$$P_{LDO3} = (4.1V - (0.975 \times 1.8V)) \times 60 \text{ mA}$$

$$P_{LDO3} = (2.35V \times 60 \text{ mA})$$

$$P_{LDO3} = 140.7 \text{ milli-Watts}$$

$$P_{LDO4} = (4.1V - (0.975 \times 1.8V)) \times 60 \text{ mA}$$

$$P_{LDO4} = 140.7 \text{ milli-Watts}$$

$$P_{TOTAL} = P_{LDO1} + P_{LDO2} + P_{LDO3} + P_{LDO4}$$

$$P_{TOTAL} = 516.4 \text{ milli-Watts}$$

## Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to air ( $\theta_{JA}$ ) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7 "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages". The standard describes the test method and board specifications for measuring the thermal resistance from junction to case. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to AN792 for more information regarding this subject.

$$T_{JRISE} = P_{TOTAL} \times \theta_{JA}$$

$$T_{JRISE} = 516.4 \text{ milli-Watts} \times 112.4^{\circ}\text{C/Watt}$$

$$T_{JRISE} = 58.1^{\circ}\text{C}$$

## Junction Temperature Estimate

To estimate the internal junction temperature ( $T_J$ ), the calculated junction temperature rise ( $T_{JRISE}$ ) is added to the ambient or offset temperature ( $T_{AMBIENT}$ ). For this example the worst case junction temperature is estimated below.

$$T_J = T_{JRISE} + T_{AMBIENT}$$

$$T_J = 108.1^{\circ}\text{C}$$

## Maximum Package Power Dissipation

The maximum power dissipation capability for the TC1307 can be approximated by finding the maximum allowable temperature rise from junction to case and dividing that by the estimated thermal resistance of the application. For this example, the maximum allowable junction temperature rise is  $125^{\circ}\text{C} - 50^{\circ}\text{C}$  or  $75^{\circ}\text{C}$ . By dividing  $75^{\circ}\text{C}$  by the estimated thermal resistance ( $112.4^{\circ}\text{C/Watt}$ ), the maximum allowable power dissipation is calculated to be 667.3 milli-Watts.

## 5.6 Device Protection

### 5.6.1 OVER CURRENT LIMIT

In the event of a faulted output load, the maximum current the LDO will permit to flow is limited internally. For each of the four LDO's internal to the TC1307, the limit in the event of a short circuit will be 360 mA typical. This limit can be used to prevent damage to the circuit board or connectors. The over current protection for each LDO output is independent. For example, if LDO1 output is shorted to ground, the over current protection will limit the output current for LDO1. If the junction temperature does not rise above the typical  $150^{\circ}\text{C}$  thermal shutdown point the other three LDO outputs (LDO2, LDO3, LDO4) will remain within regulation.

## 5.6.2 OVER TEMPERATURE PROTECTION

If the internal power dissipation within the TC1307 is excessive due to a faulted load or higher than specified line voltage, an internal temperature sensing element will prevent the junction temperature from exceeding approximately 150°C. If the junction temperature does exceed approximately 150°C, all LDO outputs will be disabled until the junction temperature cools to approximately 140°C, at which point the device will resume normal operation. The  $\overline{\text{RESET}}$  output will continue to operate normally in the event of a thermal shutdown.

## 5.7 Recommended Physical Layout

Figure 5-2 represents a typical layout using the TC1307 16-pin QSOP package.  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$  are 1  $\mu\text{F}$  X5R 0603 ceramic output capacitors and  $C_{\text{IN}}$  is a 2.2  $\mu\text{F}$  X5R 0805 ceramic capacitor. No other components are required for this quad output LDO with microcontroller reset function. Utilizing the highly integrated TC1307, the total board area required is less than 0.300 square inches.

For CMOS LDOs, the GND or quiescent current is small when compared to the maximum output current capability. The GND pins connected to the TC1307 do not carry high current and it is not necessary for them

to be wide. It is more important for the GND pins to be connected to a quiet circuit ground. Noise on the GND pins may result in noise at the output of the LDO. In Figure 5-2, a ground plane is used to connect the TC1307 Pins to the GND plane that has the  $V_{\text{OUT}}$  capacitor return tied to it. For applications that have ripple voltage on the input, the  $C_{\text{IN}}$  capacitor return can be separated from the ground plane by running a trace from the capacitor to the ground plane. This impedance will help to reduce the noise on the output of the LDO.

The output voltage regulation uses the GND pins of the TC1307 as the return path for the internal bandgap reference. Any voltage drops between the load and the respective  $V_{\text{OUT}}$  pin and GND pin will show up as regulation losses. It is important to size the  $V_{\text{OUT}}$  and GND conductors for minimum voltage drops. The maximum application load current will determine how large these traces should be. As shown in Figure 5-2, a ground plane can be used minimize the trace resistance from the load to the TC1307 GND pin.

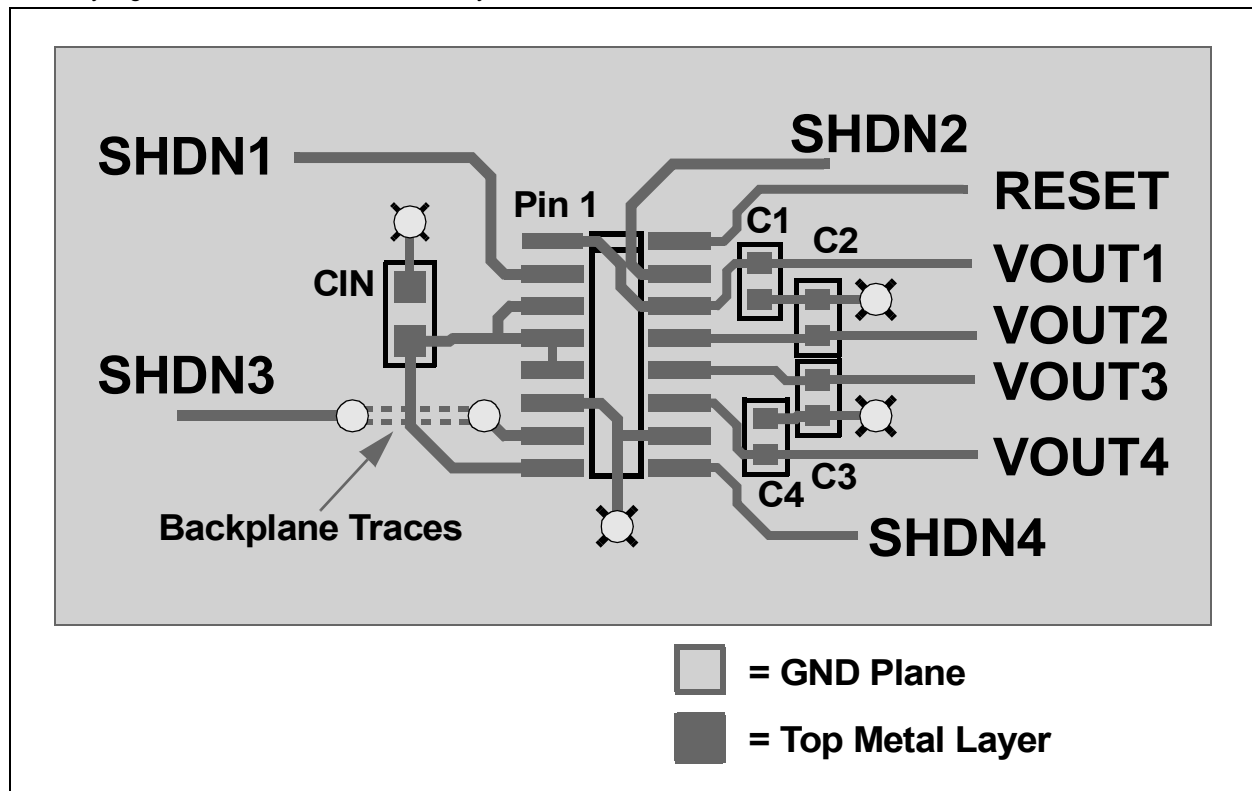


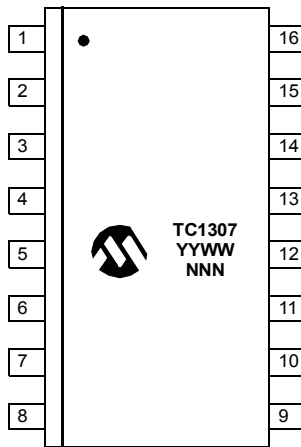
FIGURE 5-2: TC1307 Typical Layout.

# TC1307

---

## 6.0 PACKAGING INFORMATION

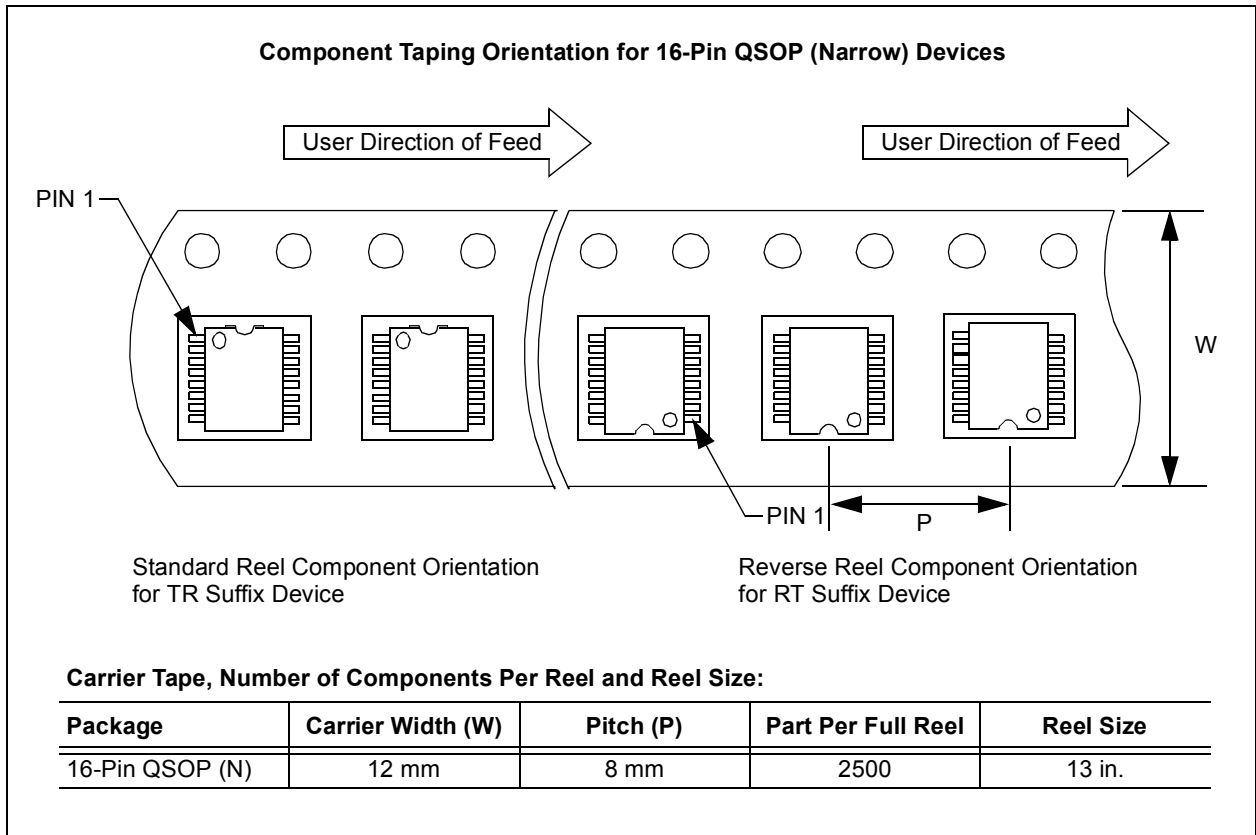
### 6.1 Package Marking Information



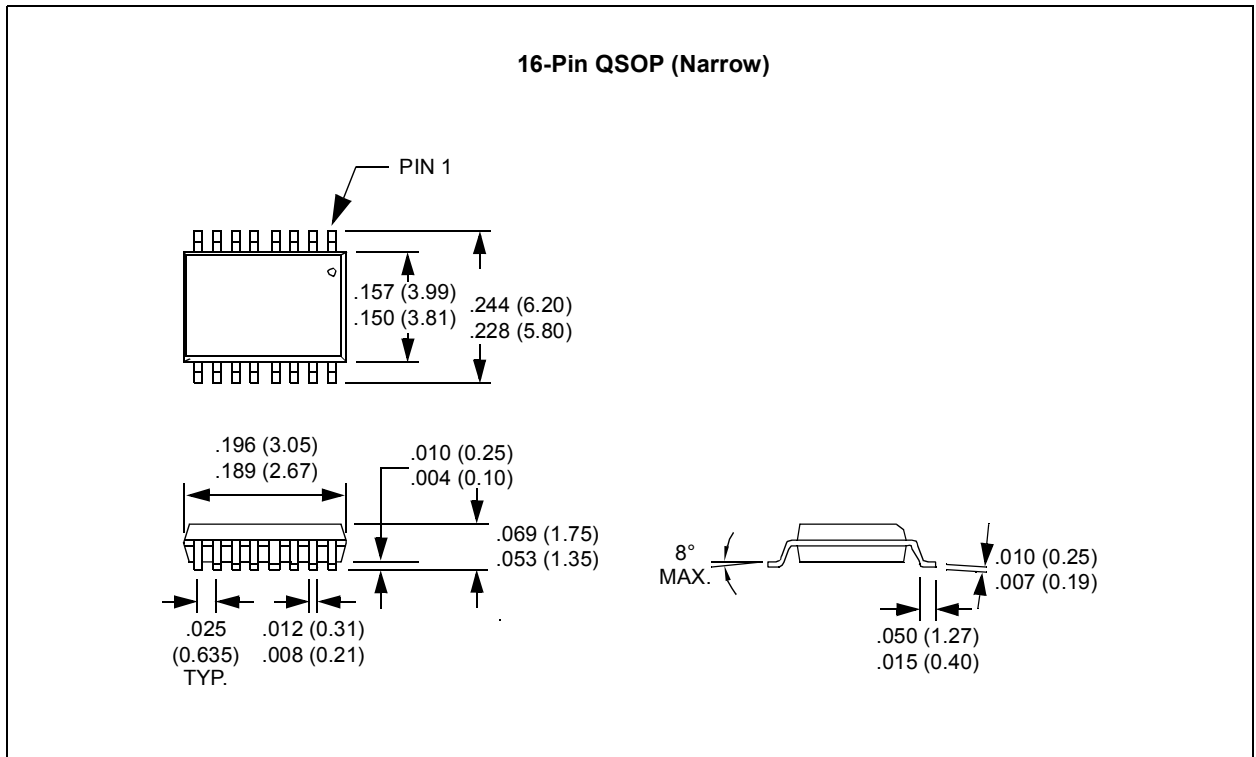
<b>Legend:</b>	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

\* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

## 6.2 Taping Form



## 6.3 Packaging Information



# TC1307

---

---

NOTES:

## ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

### Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

**[www.microchip.com](http://www.microchip.com)**

The file transfer site is available by using an FTP service to connect to:

**<ftp://ftp.microchip.com>**

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

## Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and  
1-480-792-7302 for the rest of the world.

013001

# TC1307

---

---

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager Total Pages Sent  
RE: Reader Response  
From: Name \_\_\_\_\_  
Company \_\_\_\_\_  
Address \_\_\_\_\_  
City / State / ZIP / Country \_\_\_\_\_  
Telephone: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_ FAX: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_

Application (optional):

Would you like a reply? \_\_\_Y \_\_\_N

Device: **TC1307**

Literature Number: **DS21702A**

Questions:

1. What are the best features of this document?

---

---

2. How does this document meet your hardware and software development needs?

---

---

3. Do you find the organization of this data sheet easy to follow? If not, why?

---

---

4. What additions to the data sheet do you think would enhance the structure and subject?

---

---

5. What deletions from the data sheet could be made without affecting the overall usefulness?

---

---

6. Is there any incorrect or misleading information (what and where)?

---

---

7. How would you improve this document?

---

---

8. How would you improve our software, systems, and silicon products?

---

---



## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	X	-XX	X	X	X	XX
Device	Threshold Voltage	LDO Output Voltages	Temp. Range	Packaging Type	# Leads	Tape & Reel
Device:	TC1307: 4-Channel LDO w/Select Mode, Shutdown and Independent Reset					
Threshold Voltage:	R = 2.63V					
LDO Output Voltages:	XY = 1.8V XY = 2.5V XY = 2.8V XY = 3.0V					
Temperature Range:	V = -40°C to +125°C (Extended)					
Package:	QR = QSOP Package, 16-lead					
Tape and Reel:	TR = Tape and Reel					

### Examples:

a) TC1307R-XYVQRTR

## Sales and Support

### Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site ([www.microchip.com](http://www.microchip.com))

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

### New Customer Notification System

Register on our web site ([www.microchip.com/cn](http://www.microchip.com/cn)) to receive the most current information on our products.

# TC1307

---

NOTES:

---

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

#### Trademarks

The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

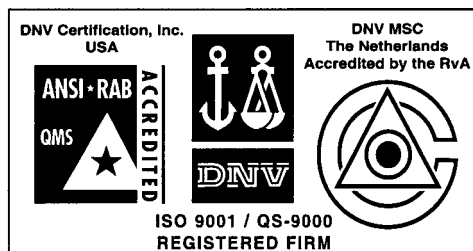
dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microID, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Term Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



*Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.*



# MICROCHIP

## WORLDWIDE SALES AND SERVICE

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200 Fax: 480-792-7277  
Technical Support: 480-792-7627  
Web Address: <http://www.microchip.com>

#### Rocky Mountain

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-692-7966 Fax: 480-792-7456

#### Atlanta

500 Sugar Mill Road, Suite 200B  
Atlanta, GA 30350  
Tel: 770-640-0034 Fax: 770-640-0307

#### Boston

2 Lan Drive, Suite 120  
Westford, MA 01886  
Tel: 978-692-3848 Fax: 978-692-3821

#### Chicago

333 Pierce Road, Suite 180  
Itasca, IL 60143  
Tel: 630-285-0071 Fax: 630-285-0075

#### Dallas

4570 Westgrove Drive, Suite 160  
Addison, TX 75001  
Tel: 972-818-7423 Fax: 972-818-2924

#### Detroit

Tri-Atria Office Building  
32255 Northwestern Highway, Suite 190  
Farmington Hills, MI 48334  
Tel: 248-538-2250 Fax: 248-538-2260

#### Kokomo

2767 S. Albright Road  
Kokomo, Indiana 46902  
Tel: 765-864-8360 Fax: 765-864-8387

#### Los Angeles

18201 Von Karman, Suite 1090  
Irvine, CA 92612  
Tel: 949-263-1888 Fax: 949-263-1338

#### New York

150 Motor Parkway, Suite 202  
Hauppauge, NY 11788  
Tel: 631-273-5305 Fax: 631-273-5335

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408-436-7950 Fax: 408-436-7955

#### Toronto

6285 Northam Drive, Suite 108  
Mississauga, Ontario L4V 1X5, Canada  
Tel: 905-673-0699 Fax: 905-673-6509

### ASIA/PACIFIC

#### Australia

Microchip Technology Australia Pty Ltd  
Suite 22, 41 Rawson Street  
Epping 2121, NSW  
Australia  
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

#### China - Beijing

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Beijing Liaison Office  
Unit 915  
Bei Hai Wan Tai Bldg.  
No. 6 Chaoyangmen Beidajie  
Beijing, 100027, No. China  
Tel: 86-10-85282100 Fax: 86-10-85282104

#### China - Chengdu

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Chengdu Liaison Office  
Rm. 2401, 24th Floor,  
Ming Xing Financial Tower  
No. 88 TIDU Street  
Chengdu 610016, China  
Tel: 86-28-6766200 Fax: 86-28-6766599

#### China - Fuzhou

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Fuzhou Liaison Office  
Rm. 531, North Building  
Fujian Foreign Trade Center Hotel  
73 Wusi Road  
Fuzhou 350001, China  
Tel: 86-591-7557563 Fax: 86-591-7557572

#### China - Shanghai

Microchip Technology Consulting (Shanghai)  
Co., Ltd.  
Room 701, Bldg. B  
Far East International Plaza  
No. 317 Xian Xia Road  
Shanghai, 200051  
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

#### China - Shenzhen

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Shenzhen Liaison Office  
Rm. 1315, 13/F, Shenzhen Kerry Centre,  
Renminnan Lu  
Shenzhen 518001, China  
Tel: 86-755-2350361 Fax: 86-755-2366086

#### Hong Kong

Microchip Technology Hongkong Ltd.  
Unit 901-6, Tower 2, Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2401-1200 Fax: 852-2401-3431

#### India

Microchip Technology Inc.  
India Liaison Office  
Divyasree Chambers  
1 Floor, Wing A (A3/A4)  
No. 11, O'Shaughnessey Road  
Bangalore, 560 025, India  
Tel: 91-80-2290061 Fax: 91-80-2290062

### Japan

Microchip Technology Japan K.K.  
Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa, 222-0033, Japan  
Tel: 81-45-471-6166 Fax: 81-45-471-6122

### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea 135-882  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore, 188980  
Tel: 65-334-8870 Fax: 65-334-8850

### Taiwan

Microchip Technology Taiwan  
11F-3, No. 207  
Tung Hua North Road  
Taipei, 105, Taiwan  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### Denmark

Microchip Technology Nordic ApS  
Regus Business Centre  
Lautrup høj 1-3  
Ballerup DK-2750 Denmark  
Tel: 45 4420 9895 Fax: 45 4420 9910

#### France

Microchip Technology SARL  
Parc d'Activite du Moulin de Massy  
43 Rue du Saule Trapu  
Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

#### Germany

Microchip Technology GmbH  
Gustav-Heinemann Ring 125  
D-81739 Munich, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

#### Italy

Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Taurus 1 V. Le Colleoni 1  
20041 Agrate Brianza  
Milan, Italy  
Tel: 39-039-65791-1 Fax: 39-039-6899883

#### United Kingdom

Arizona Microchip Technology Ltd.  
505 Eskdale Road  
Winnersh Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44 118 921 5869 Fax: 44-118 921-5820

01/18/02

